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HONEYWELL INC HOPKINS MN DEFENSE SYSTEMS DIV
DEVELOPMENT OF TWO MONOLITHIC INTEGRATED CIRCUITS AND A 10-KHZ --ETC(U)
FEB 79 B GOBLISH, K CEOLA

F/G 19/1

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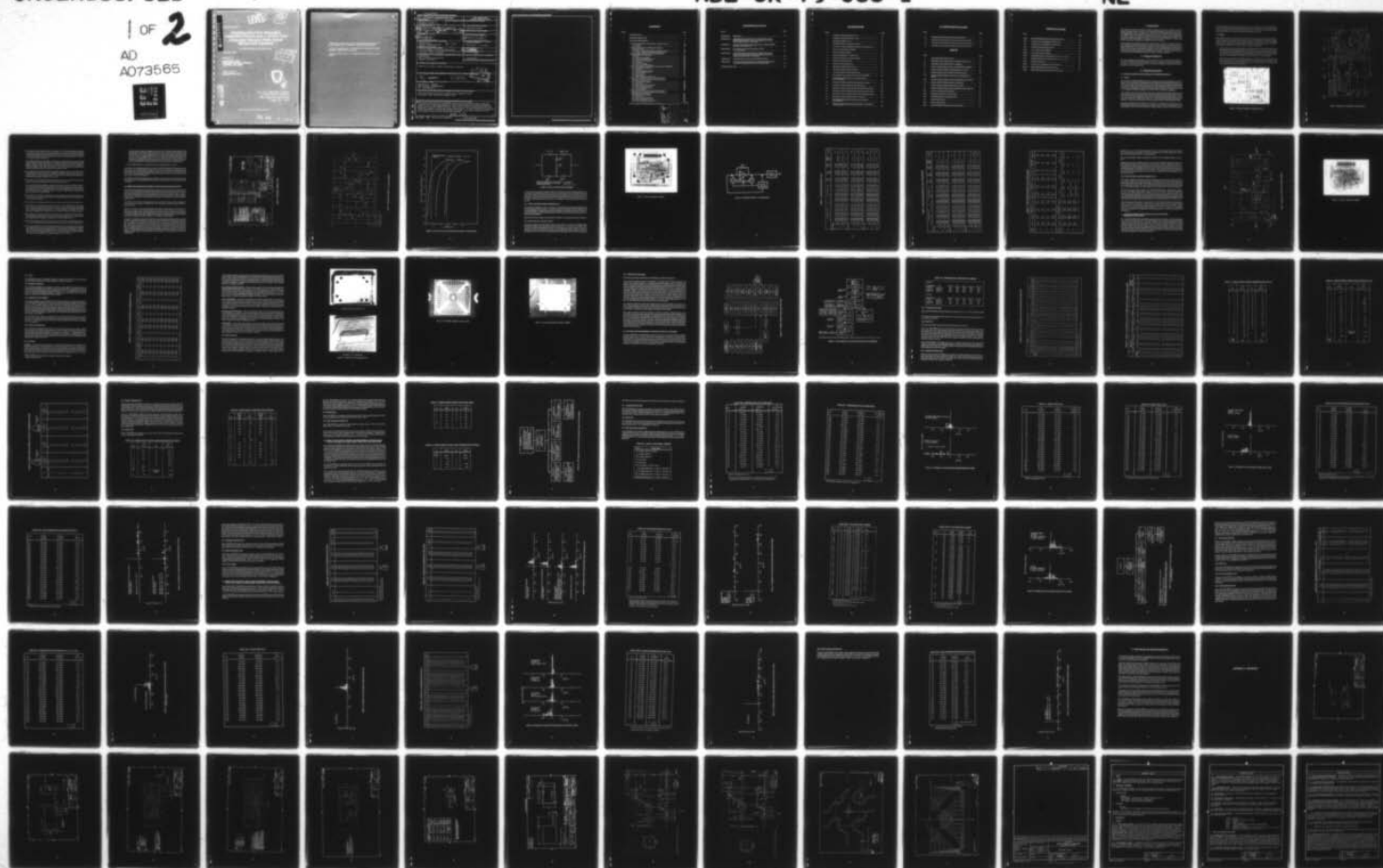
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1. Introduction

The program to develop two bipolar monolithic integrated circuits was initiated in 1976 by Honeywell, Defense Systems Division, in an independent development program. One of the monolithic integrated circuits was designed as a replacement for the interface hybrid microcircuit, PN 10990455. The other monolithic integrated circuit would be used in a cost-reduced hybrid microcircuit oscillator to replace the 10-kHz hybrid microcircuit oscillator, PN 11711427. Completion of the development effort was included as a task in contract DAAG39-77-C-0056 for the DT/OT-II quantity of XM587E2 and XM724 electronic time fuzes.

The development of two bipolar monolithic integrated circuits and a low cost 10-kHz Tape Automatic Bonded (TAB) Hybrid Microcircuit Oscillator (HMO) comprised the following areas: (1) design and fabrication of two monolithic integrated circuits; (2) electrical testing of the two integrated circuits; (3) design and fabrication of the prototype 10-kHz TAB HMOs; (4) electrical and environmental testing of the prototype TAB HMOs; (5) fabrication, electrical testing, and environmental testing of TAB HMOs utilizing the phase II monolithic amplifier.

2. Program Objective

The primary program objective was to reduce the production cost of the existing two hybrid circuits for the XM587E2 and XM724 electronic time fuzes, through the use of silicon monolithic technology to replace the individual device, chip-and-wire assembly techniques presently employed in these two hybrid circuits.

3. Detailed Description

3.1 DESIGN AND FABRICATION OF MONOLITHIC INTEGRATED CIRCUITS

3.1.1 General

The interface monolithic integrated circuit die topology and the circuit schematic are shown in figures 1 and 2, respectively. The interface circuit was tested at room ambient. Some limited temperature testing was performed, but the effort was terminated prior to complete testing because the parasitic voltages, even at ambient temperatures, were considered excessive. The following is a list of problems isolated prior to termination along with planned solutions. References are made to the monolithic interface specification 11711670, which is contained in appendix A.

After completion of a worst case analysis, the layout was initiated. Nickel silicide Schottky diodes were selected to float the substrate, rather than the standard platinum silicide diodes, to minimize the forward drop. Processing problems were encountered and attributed to the nickel silicide. The manufacturer decided that it would be too costly to develop the nickel silicide process; therefore, a lot of parts was fabricated with the standard platinum silicide Schottky diodes.

Ten parts were fabricated and subjected to evaluation. As anticipated, firing the silicon controlled rectifier (SCR) resulted in catastrophic failure and would have to be eliminated by metal mask changes. The circuit was functional in the XM587 system (exclusive of the SCR); however,

parasitic voltages at pins which should have been low were considered excessive. Design changes were proposed which should clamp these parasitic voltages to a predictable and acceptable value; however, the effort was terminated as sufficient progress had been made by the Harry Diamond Laboratories (HDL) in an alternative design using dielectric isolation.

3.1.2 Details

The interface circuit was tested at room ambient. Some limited temperature testing was performed, but the effort was terminated prior to complete testing because the parasitic voltages, even at ambient temperatures, were considered excessive. The following is a list of problems isolated prior to termination along with proposed solutions. References are made to the monolithic interface specification 11711670, which is contained in appendix A.

- 1) Arsenic resistors were designed assuming a 6-Vdc breakdown. Normally, the voltage across the arsenic resistors in typical designs are a few tenths of a volt. The 6-Vdc limit was based on the lowest expected breakdown from available processing information. Based on interface test results, the resistors had an actual breakdown voltage of 5.4 Vdc, and two resistors, R3 and R16, were proposed for redesign to accommodate this lower breakdown.
- 2) Resistor R3 was designed as a floating resistor to accommodate testing. This resistor would have to be tied down, and the testing would have to be modified because interface testing results indicated a parasitic SCR could result from this floating resistor. The parasitic action would not occur with R3 tied down.

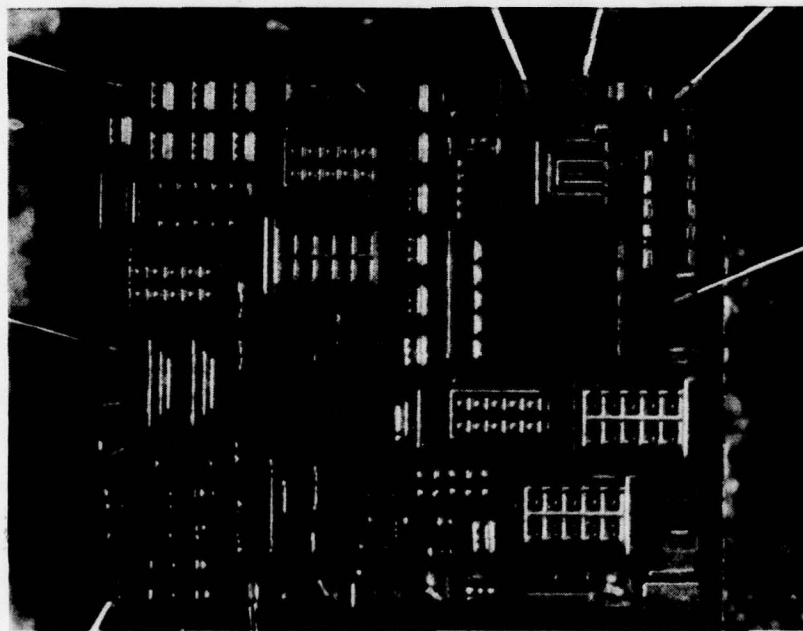


Figure 1. Interface monolithic integrated circuit.

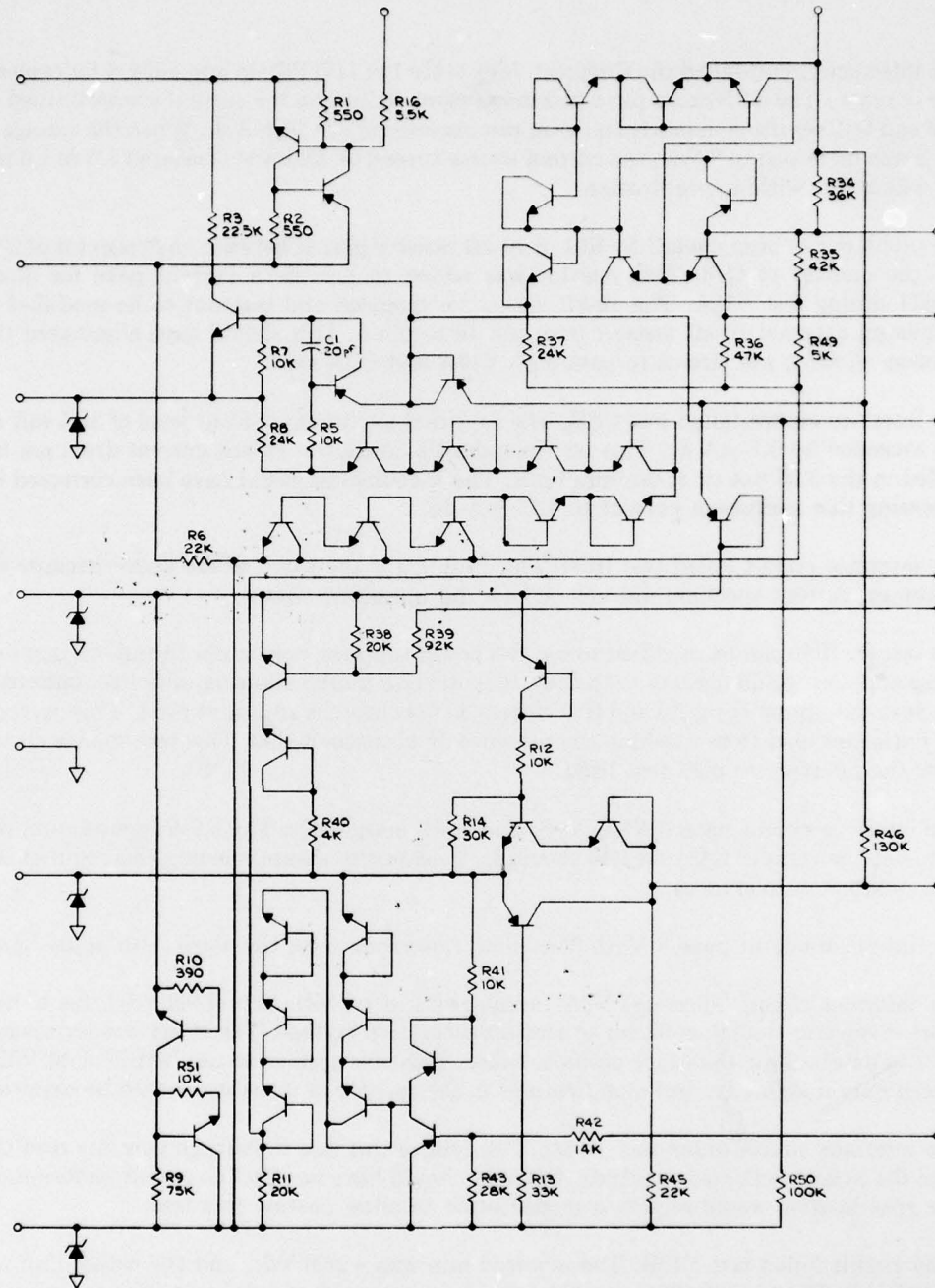


Figure 2. Schematic of monolithic interface circuit.

- 3) The interface circuit failed the CSA test. (See table 1 of 11711670 in appendix A for exploration of tests.) The 3.0 Vdc on pin 5 was insufficient to turn on the current source formed by Q18 and Q19 resulting in less than the minimum current of 1.05 mA dc. When the voltage at pin 5 was increased to 9 Vdc, the current source turned on and was measured 1.5 to 1.6 mA dc, which was within specification.

The problem has been caused by R51, a 10-k Ω resistor placed between the collector of Q19 and the emitter of Q18. This resistor was added to provide a current path for diode QCR11 during test V16A. The 10-k Ω was to be removed and test was to be modified to include an external 10-k Ω resistor from pin 16 to pin 5. This should have eliminated the problem allowing the circuit to pass both V16A and CSA tests.

- 4) The interface circuit failed test CSB. The specified maximum current level of 3.05 mA dc was exceeded by 0.7 mA dc. This test includes the initializer circuit current drain not included in the 3.05 mA dc maximum limit. The specification could have been corrected by increasing this maximum current to 4.15 mA dc.
- 5) The interface circuit failed test IR50. This problem is the same as the above because the maximum current specified did not include the initializer circuit.

The test for IR50 can be modified to use two power supplies, one on pin 13 and one on pin 1. These supplies would operate so that QCR2 is reverse biased allowing initializer current to flow into the supply at pin 13 and R50 current to flow into the supply at pin 1. This prevents the initializer load from masking the presence or absence of R50. This test change should allow the interface to pass test IR50.

- 6) The interface circuit passed V9A, V9B, and V9C, marginally. The 3.6-Vdc minimum was met, but the ratio of R45 and R46 should be modified to assure meeting this requirement over production tolerances.
- 7) The interface circuit passed V9B. The same comments from the above also apply here.
- 8) The interface circuit failed test V8AD (required min 1.0 Vdc, actual 0.9 Vdc) due to high resistor value or to high collector to emitter saturation voltage. The effort was terminated prior to determining the exact problem cause. This also applied to test V8BD. Test V8BD passed only marginally, and modifications to the resistor or transistor would be required.
- 9) The interface circuit failed test V16A. This failure was due to leakage currents resulting from the Schottky floated substrate, but they should have no effect on circuit performance. The specification would require a modification to allow passing this test.
- 10) The circuit failed test V13B. The required min was -26.0 Vdc, and the actual min was -25.7 Vdc. The diode QCR11 would have to be increased in size to meet this requirement.
- 11) The circuit failed test V3A. This test establishes the maximum voltage that can be reached on the firing capacitor prior to arming and is the main reason for terminating the interface effort. The fuze system holds an approximately 1-k Ω load on the capacitor prior to arming. With this 1-k Ω load, the parasitic level for V3A was approximately -200 mVdc. Without the 1-k Ω load (as specified), the voltage increased to -1 to -2 Vdc.

The voltage was caused by leakage current due to the Schottky floated substrate. This leakage current was 1.6 and 3.8 μA dc at 71° and 125°C, respectively. The firing capacitor does not have a 1-k Ω load for approximately 0.5 s during the setting cycle, which would result in a capacitor voltage of 360 mVdc at 71°C. This is not a predictable leakage current and may vary considerably from lot to lot. This voltage could be actively clamped by a transistor to provide a predictable voltage level on the order of 0.3 Vdc; however, the project was terminated due to acceptable progress on the competitive interface effort.

- 12) The SCR would have to be placed off chip to handle the heavy currents.

In summary, the basic design approach of using low drop Schottky diodes to float the device substrate results in excessive parasitic voltages. These could be eliminated by implementing the same design with a conventional dielectrically isolated process; however, the chip cost would be more. The Schottky float approach had not been previously attempted and, if acceptable, would have been a most effective approach.

The possibility of fabricating this design with a dielectric isolation process should be investigated. With this process, it is conceivable that all components could be placed on chip, resulting in a low cost device.

3.2 DESIGN AND FABRICATION OF MONOLITHIC AMPLIFIER INTEGRATED CIRCUIT

The monolithic amplifier characteristics shown in figure 3 were based on a worst case analysis of the twin-T network combined with the oscillator hybrid circuit required performance. On a worst case basis over temperature, the twin-T network can contribute a frequency error of approximately 40 Hz. This provides a total allowable amplifier error of approximately 18 Hz in order to remain within specification. This 18-Hz figure was utilized to establish the monolithic amplifier characteristics.

The shaper circuit of figure 4 provides the rise times required to interface with the complementary metal oxide semiconductor (CMOS) scaler. Also, hysteresis is provided to prevent chatter at the switch point.

Figure 5 is a plot of the twin-T network feedback attenuation versus frequency for the twin-T network shown in figure 6. The three plots are calculated for nominal, minimum, and maximum twin-T network attenuations. The phase shift across the twin-T network anywhere on these plots is 180 deg. Therefore, as long as the amplifier gain is equal to or greater than the twin-T network attenuation, oscillations can exist. Figure 4 is a schematic of the amplifier.

The amount of change in frequency of oscillation versus a change in phase through the monolithic amplifier is greatly reduced as the trim point forces the twin-T network into regions of increasing loss. A compromise is necessary since increasing twin-T network loss requires higher amplifier gain, which results in errors due to excessive phase shift at the operating frequency. A minimum gain of 35.5 dB was selected for twin-T network trimming as the optimum compromise, allowing 2 deg of amplifier phase shift at the operating frequency, resulting in a sensitivity of frequency drift due to amplifier phase shift of approximately 8 Hz/deg phase shift. These parameters assure meeting oscillator hybrid circuit performance characteristics over temperature for worst case considerations.



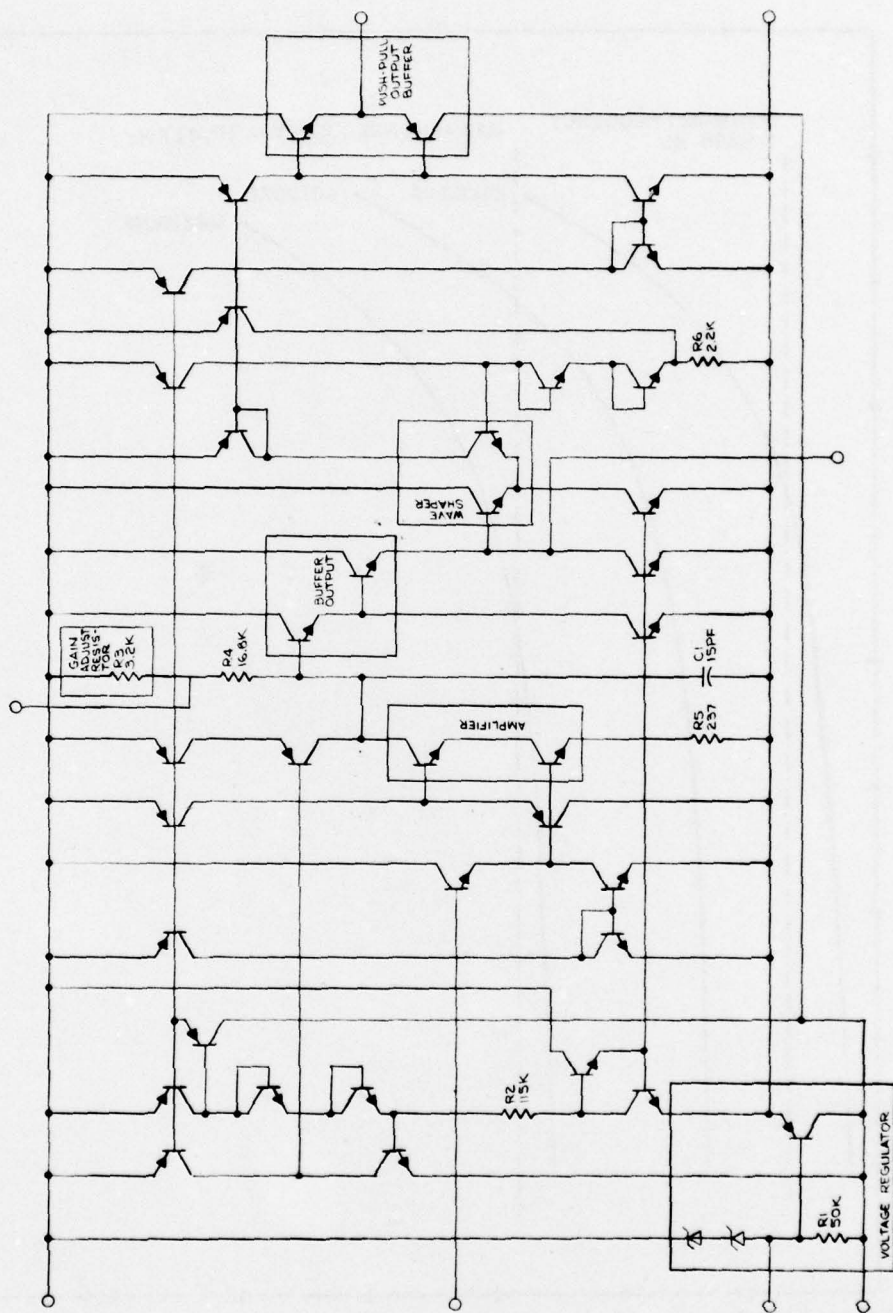


Figure 4. Schematic of Phase I monolithic amplifier.

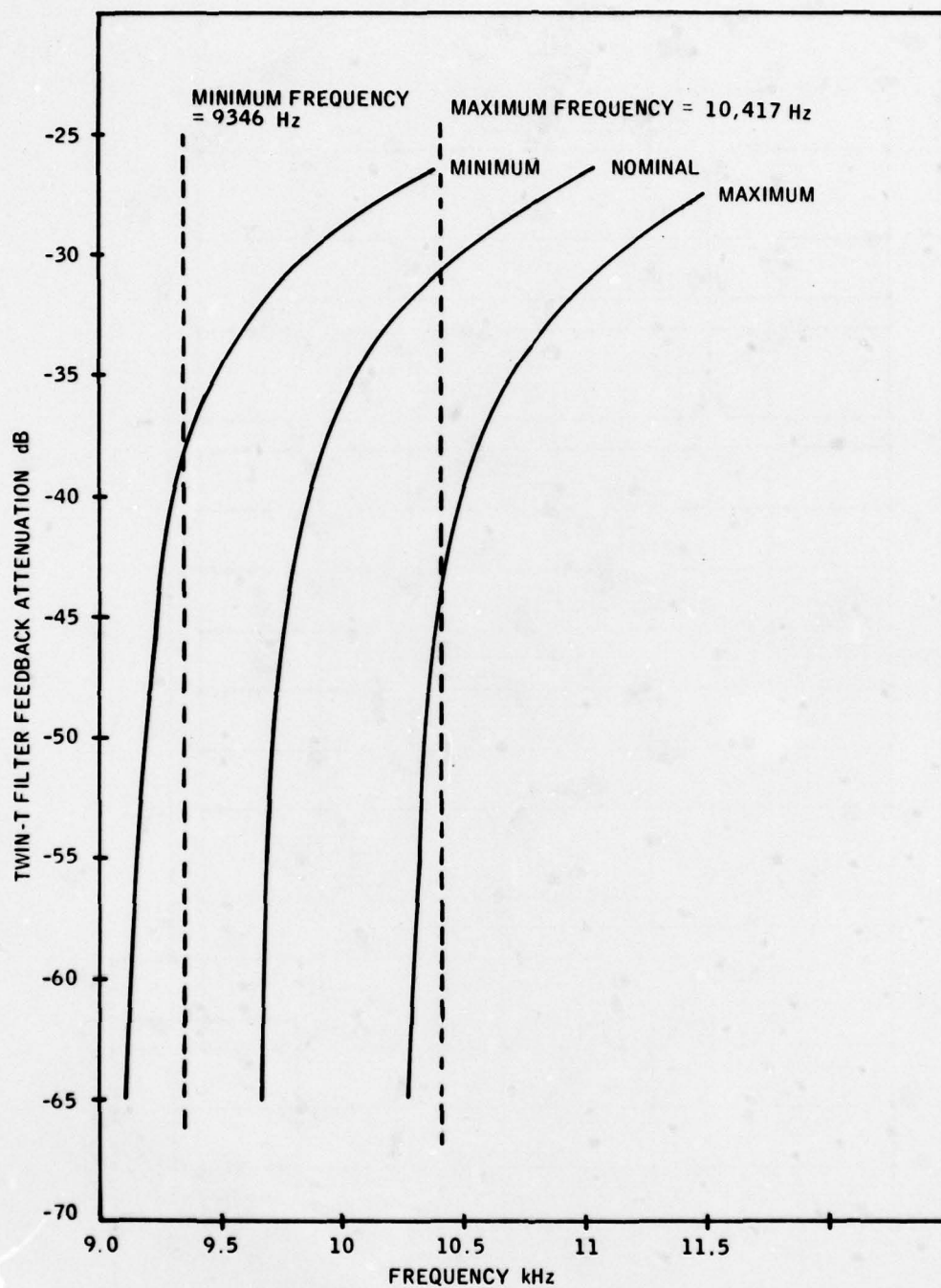


Figure 5. Plot of twin-T network feedback attenuation versus frequency.

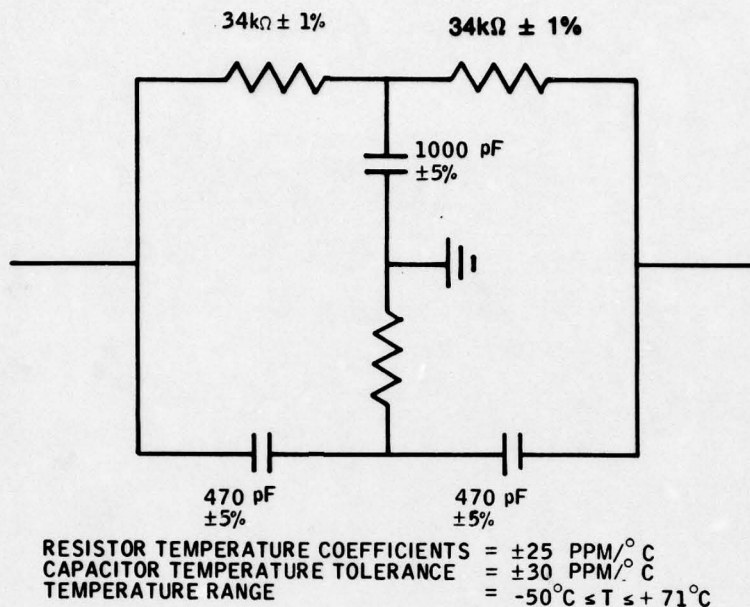


Figure 6. Twin-T network schematic diagram.

The amount of excess gain also effects stability, but instability is held to an insignificant level by limiting the amount of excess gain. This is limited by trimming the twin-T network until oscillations cease, which indicates that the amplifier gain is just slightly less than the twin-T network attenuation. A ground path then removed from the integrated circuit increases the gain by 1.5 dB. This 1.5-dB excess gain has been shown to be adequate to assure start-up without affecting stability.

3.2.1 Phase I. Monolithic Amplifier Integrated Circuit

The monolithic amplifier is a $1.6 \times 1.9 \text{ mm}$ ($63 \times 75 \text{ mil}$) bipolar monolithic integrated circuit. The die topology is shown in figure 7. Conventional bipolar processing is utilized to fabricate the monolithic amplifier, with the exception of an ion implant step to obtain the resistors. Production should not present a problem for any manufacturer with a reasonable bipolar process and compatible design guidelines.

Electrical data were obtained on the monolithic amplifier in the configuration shown in figure 8.

The electrical data are contained in table I.

Monolithic amplifier test data indicate excessive phase shift over voltage, the specified phase shift being 0.15 deg, while actual measurements range from 0.2 to 0.4 deg. This is a difficult measurement to make since the absolute accuracy of the equipment is 2 deg. A properly tuned oscillator will produce a shift in frequency of approximately 6.2 Hz/deg of phase shift for a total shift of 2.5 Hz from -21.5 to -30 V for a 0.4-deg change in amplifier phase. This is a $0.025\text{-}\mu\text{s}$ change in

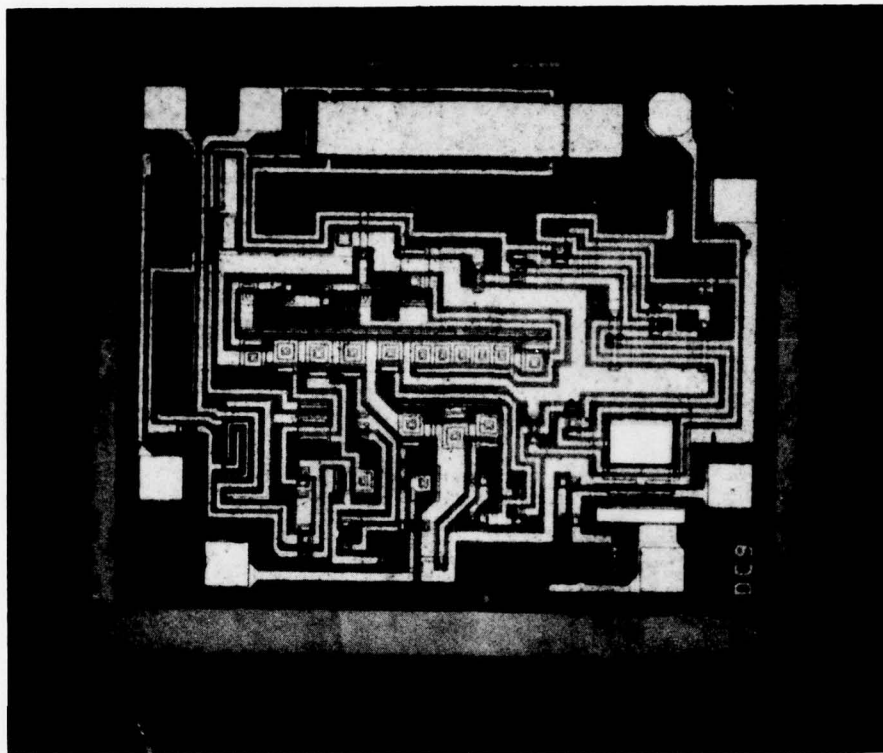


Figure 7. Phase I monolithic amplifier.

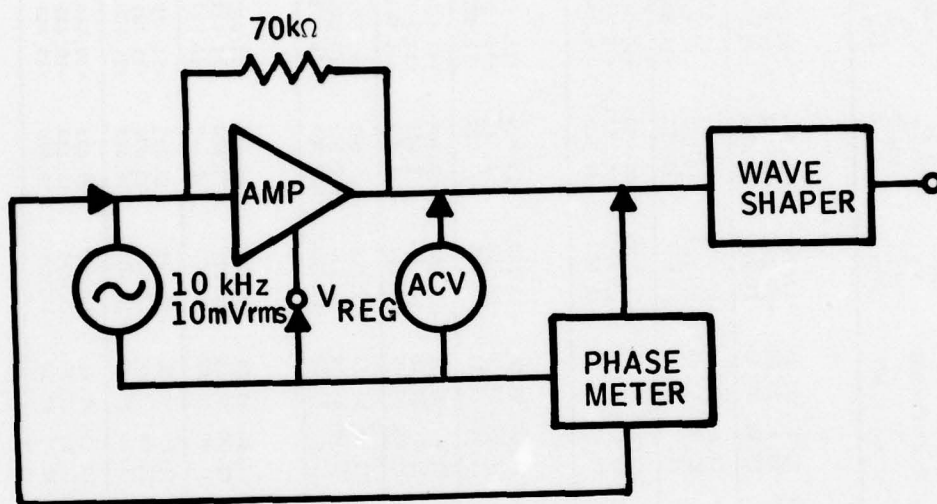


Figure 8. Monolithic amplifier, test configuration.

TABLE I. AMPLIFIER ELECTRICAL DATA

Device #93												
With Short Circuit				Without Short Circuit				V _{dc} V _Z Pin 7 to grd	V _{dc} V _{reg} Pin 2 to grd	V _{dc} V _{dc} out Pin 1 to grd	No Bias R _{50k} Pin 6 to Pin 7	Pos. lead on #7
E _{in}	E ₀₁	A _v	dB	E _{in}	E ₀₂	A _v	dB					
-17	0.0071	0.4301	60.57	35.64	0.0070	0.5047	72.1	37.16	-13.311	-12.654	-11.007	#93 Rt
-21	0.0070	0.4335	61.93	35.84	0.0070	0.5069	72.4	37.20	-13.357	-12.709	-11.091	
-30	0.0070	0.4326	61.80	35.82	0.0070	0.5059	72.27	37.18	-13.495	-12.854	-11.219	
-17	0.0070	0.4322	61.74	35.81	0.0070	0.5017	71.67	37.11	-13.501	-12.907	-11.426	+71°C Rt
-21	0.0070	0.4327	61.67	35.80	0.0070	0.5045	72.07	37.15	-13.540	-12.957	-11.460	
-30	0.0070	0.4312	61.60	35.79	0.0070	0.5039	71.98	37.14	-13.667	-13.093	-11.591	
-17	0.0070	0.4285	61.21	35.73	0.0070	0.5038	71.97	37.14	-12.9062	-12.1154	-10.1930	-55°C Rt
-21	0.0070	0.4362	62.31	35.89	0.0070	0.5109	72.98	37.26	-12.9566	-12.1654	-10.2171	
-30	0.0071	0.4342	62.00	35.85	0.0070	0.5087	72.67	37.23	-13.087	-12.301	-10.374	
Device #89												
-17	0.0070	0.4268	60.97	35.70	0.0070	0.5002	71.46	37.08	-13.274	-12.620	-11.067	#89 Rt
-21	0.0070	0.4308	61.54	35.78	0.0070	0.5046	72.07	37.15	-13.324	-12.685	-11.103	
-30	0.0070	0.4298	61.40	35.76	0.0070	0.5033	71.90	37.13	-13.455	-12.827	-11.255	
-17	0.0070	0.4246	60.66	35.66	0.0070	0.4970	71.0	37.02	-13.480	-12.909	-11.509	+71°C Rt
-21	0.0070	0.4285	61.21	35.74	0.0070	0.5012	71.6	37.10	-13.588	-12.950	-11.517	
-30	0.0070	0.4281	61.16	35.73	0.0070	0.5004	71.48	37.08	-13.744	-13.084	-11.681	
-17	0.0070	0.4340	61.16	35.73	0.0069	0.5092	72.74	37.23	-12.880	-12.097	-10.207	-52°C Rt
-21	0.0070	0.4341	62.01	35.84	0.0070	0.5093	72.76	37.24	-12.934	-12.154	-10.245	
-30	0.0070	0.4330	61.86	35.83	0.0069	0.5082	72.6	37.22	-13.058	-12.284	-10.395	
Device #90												
-17	0.0070	0.4265	60.93	35.70	0.0070	0.5000	71.43	37.08	-13.267	-12.623	-11.049	#90 Rt
-21	0.0070	0.4307	61.53	35.78	0.0070	0.5044	72.06	37.15	-13.318	-12.682	-11.115	
-30	0.0070	0.4291	61.30	35.75	0.0069	0.5028	72.86	37.12	-13.433	-12.807	-11.227	
-17	0.0070	0.4249	60.70	35.66	0.0070	0.4975	71.07	37.03	-13.465	-12.891	-11.479	+71°C Rt
-21	0.0070	0.4288	61.26	35.74	0.0070	0.5015	71.64	37.10	-13.504	-12.939	-11.491	
-30	0.0070	0.4270	61.0	35.71	0.0070	0.4998	71.40	37.07	-13.606	-13.049	-11.630	
-17	0.0070	0.4345	62.10	35.86	0.0070	0.5097	72.81	37.24	-12.878	-12.096	-10.190	-52°C Rt
-21	0.0070	0.4345	62.10	35.86	0.0069	0.5097	73.87	37.37	-12.935	-12.156	-10.245	
-30	0.0070	0.4336	61.94	35.84	0.0070	0.5010	72.71	37.23	-13.032	-12.259	-10.349	

TABLE I. AMPLIFIER ELECTRICAL DATA (CONTINUED)

With Short Circuit		Without Short Circuit		V _{dc} V _Z Pin 7 to grd	V _{dc} V _{reg} Pin 2 to grd	V _{dc} V _{dc} out Pin 1 to grd	No Bias R _{50K} Pin 6 to Pin 7	Pos. lead on #7
E _{in}	E ₀₁	A _v	dB	E _{in}	E ₀₂	A _v	dB	
Device #91								
-17	0.0070	0.4260	60.86	35.69	0.0070	0.4992	71.31	37.06
-21	0.0070	0.4322	61.74	35.81	0.0070	0.5057	72.24	37.17
-30	0.0070	0.4296	61.37	35.76	0.0070	0.5029	71.84	37.13
+71°C								
-17	0.0076	0.4245	60.85	35.68	0.00700	0.4966	70.94	37.02
-21	0.0076	0.4284	60.68	35.66	0.00700	0.5008	71.54	37.09
-30	0.0076	0.4276	60.57	35.64	0.00700	0.5000	71.43	37.08
-55°C								
-17	0.0075	0.4337	61.52	35.78	0.00700	0.5083	72.61	37.22
-21	0.0076	0.4337	61.43	35.77	0.00700	0.5084	72.63	37.22
-30	0.0075	0.4321	61.29	35.75	0.00700	0.5069	72.41	37.20
Device #97								
-17	0.00705	0.4299	60.70	35.70	0.00699	0.5024	71.88	37.12
-21	0.00705	0.4287	60.80	35.68	0.00699	0.5019	71.80	37.13
-30	0.00704	0.4311	61.23	35.74	0.00699	0.5043	72.14	37.16
+71°C								
-17	0.00704	0.4347	61.75	35.81	0.00699	0.5023	71.86	37.13
-21	0.00705	0.4258	60.40	35.62	0.00700	0.4982	71.17	37.05
-30	0.00705	0.4293	60.89	35.69	0.00700	0.5018	71.68	37.11
-55°C								
-17	0.00705	0.4301	61.00	35.71	0.00700	0.5040	72.0	37.15
-21	0.00705	0.4347	61.66	35.80	0.00700	0.5094	72.77	37.24
-30	0.00705	0.4333	61.46	35.77	0.00700	0.5079	72.56	37.21
Device #99								
-17	0.00705	0.4306	61.08	35.72	0.00700	0.5042	72.03	37.15
-21	0.00705	0.4368	61.96	35.84	0.00699	0.5110	73.10	37.29
-30	0.00705	0.4330	61.42	35.76	0.00699	0.5069	72.52	37.21
+71°C								
-17	0.00705	0.4290	60.85	35.68	0.00700	0.5020	71.71	37.11
-21	0.00705	0.4348	61.67	35.80	0.00699	0.5081	72.56	37.22
-30	0.00705	0.4316	61.22	35.74	0.00699	0.5049	72.23	37.17
-55°C								
-17	0.00704	0.4383	62.26	35.88	0.00698	0.5142	73.67	37.34
-21	0.00705	0.4388	62.24	35.88	0.00699	0.5144	73.59	37.34
-30	0.00704	0.4371	62.09	35.86	0.00699	0.5127	73.35	37.31

TABLE I. AMPLIFIER ELECTRICAL DATA (CONCLUDED)

Device No.	Temp	Rise Time			Fall Time			Time High		
		-17 V	-21 V	-30 V	-17 V	-21 V	-30 V	-17 V	-21 V	-30 V
93	Rt	0.35	0.3	0.3	0.35	0.3	0.3	52	52	52
	-55°C	0.3	0.3	0.3	0.25	0.25	0.25	50	50	50
	+71°C	0.2	0.2	0.2	0.2	0.2	0.2	54	54	54
94	Rt	0.3	0.3	0.3	0.3	0.3	0.25	51	51	51
	-55°C	0.3	0.3	0.28	0.3	0.3	0.25	46	46	46
	+71°C	0.3	0.3	0.3	0.3	0.3	0.3	53	53	53
96	Rt	0.5	0.5	0.5	0.3	0.3	0.3	50	50	50
	-55°C	0.5	0.5	0.45	0.25	0.25	0.25	44	44	43
	+71°C	0.5	0.5	0.45	0.25	0.25	0.25	53	53	53
98	Rt	0.3	0.3	0.25	0.3	0.3	0.25	52	52	52
	-55°C	0.25	0.25	0.25	0.3	0.25	0.3	50	50	50
	+71°C	0.28	0.28	0.25	0.3	0.3	0.28	54	54	54

Device No.	Temp	Phase Shift			at -17 V			at -21 V			at -30 V		
		-17 V	-21 V	-30 V	Rt → +71	Rt → -55	Rt → +71	Rt → -55	Rt → +71	Rt → -55	Rt → +71	Rt → -55	
93	Rt	179.1	179.1	179.4	Rt → +71	Rt → -55	Rt → +71	Rt → -55	Rt → +71	Rt → -55	Rt → +71	Rt → -55	
	-55°C	179.8	179.4	179.7	-0.7	+0.7	-0.2	+0.3	-0.3	+0.3	-0.3	+0.3	
	+71°C	178.4	178.9	179.1									
94	Rt	180.9	180.8	180.7	-0.7	-0.3	-0.8	-0.3	+0.2	-0.3			
	-55°C	180.6	180.5	180.4	Voltage phase drift = 0.2°								
	+71°C	181.1	181.0	180.9									
96	Rt	179.1	179.2	179.6	+0.2	+0.4	-0.2	+0.3	-0.4	0			
	-55°C	179.5	179.5	179.6	Voltage phase drift = 0.5°								
	+71°C	178.9	179.0	179.2									
98	Rt	179.0	179.1	179.4	-0.2	+0.5	-0.2	+0.3	-0.3	+0.2			

period from -21.5 to -30 V versus an allowance of $0.015 \mu\text{s}$. Actual oscillator data do not confirm these calculations since the drift in period over voltage has been within specification, casting doubt on the accuracy of the 0.2- to 0.4-deg readings.

The gain and regulated voltage measurements indicated that the amplifier design was acceptable.

Additional testing of the monolithic amplifier in the 10-kHz TAB HMO configuration revealed a high frequency oscillation when inducing a particular failure mode. A 200-kHz oscillation occurred when the 470-pF capacitor located near the amplifier input was removed from the circuit. A detailed analysis at the breadboard level isolated the cause of the high frequency oscillation to a positive feedback from the shaper circuit output back to the analog input. Single point failures of the oscillator cannot be allowed to result in a frequency oscillation because a hazardous system situation may result.

3.2.2 Phase II. Monolithic Amplifier Integrated Circuit

The Phase II amplifier is identical to the Phase I amplifier, with one exception. The output of the wave shaper is picked off the opposite transistor of the differential pair. This pickoff changed the phase of the shaper circuit output so that negative feedback from the shaper circuit output back to the analog input existed. This change eliminated the high frequency failure made discussed above. The schematic diagram is shown in figure 9. The topology of the die is shown in figure 10.

The Phase II amplifier was evaluated in the TAB HMO configuration. The 200-kHz oscillation did not occur while inducing failure modes in the twin-T network. Additional testing was performed which showed that 0.9- to 1.3-dB excess gain exists when the oscillator twin-T network is trimmed properly. These tests were performed at the substrate level prior to encapsulation utilizing a Model 25 ESI laser with a 0.05-mm (2-mil) bite. It is important that approximately 1.0-dB excess gain exist to assure start-up of the oscillator at voltage levels between -17.0 and -30 Vdc.

After encapsulating the oscillator, it was noted that a loss of the shield connection caused the oscillator to run at a lower frequency. It appears that a negative feedback situation exists such that the excess gain is not sufficient to assure proper operation. This was not considered a serious condition with the present encapsulating configuration. However, if changes in the packaging concept are considered, a thorough evaluation should be performed to assure proper operation of the oscillator.

3.3 DESIGN AND FABRICATION OF PROTOTYPE 10-kHz TAB HYBRID MICROCIRCUIT OSCILLATOR

The 10-kHz TAB HMO utilizes monolithic integrated circuit technology, thick film technology, tape chip-carrier technology (TCC), and TAB technology. The basic functional building blocks consist of a twin-T network and a monolithic amplifier. The monolithic amplifier is a custom designed amplifier fabricated by Motorola. The twin-T network utilized Tetrinox™ film resistors and NPO ceramic chip capacitors. Interconnection from the monolithic amplifier to the thick film conductors are formed by utilizing TCC and TAB technology. Platinum and silver thick film conductors are used to form interconnections between all other circuit elements. Drawings which document the design are contained in appendix A.

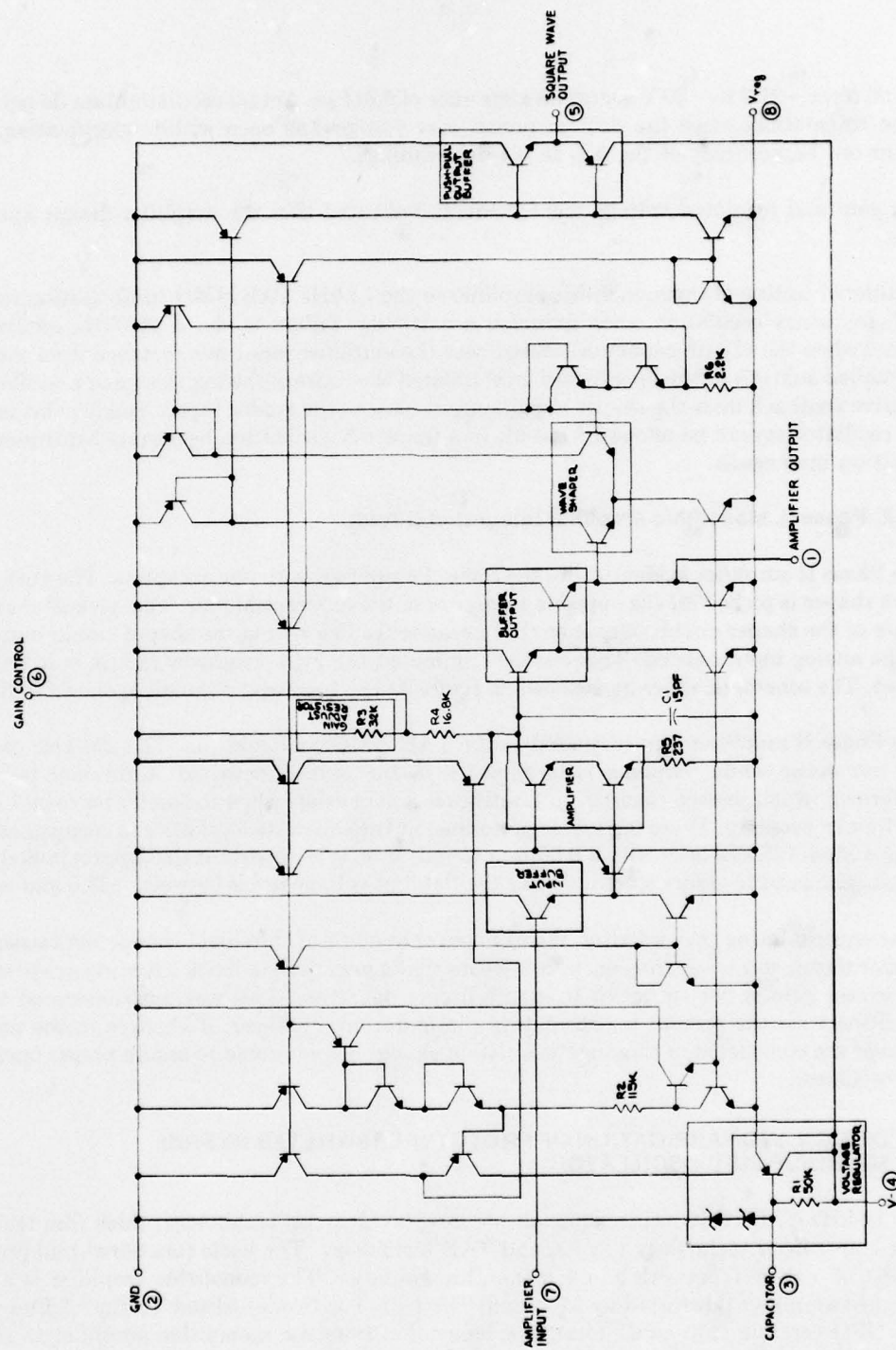


Figure 9. Schematic of Phase II monolithic amplifier.

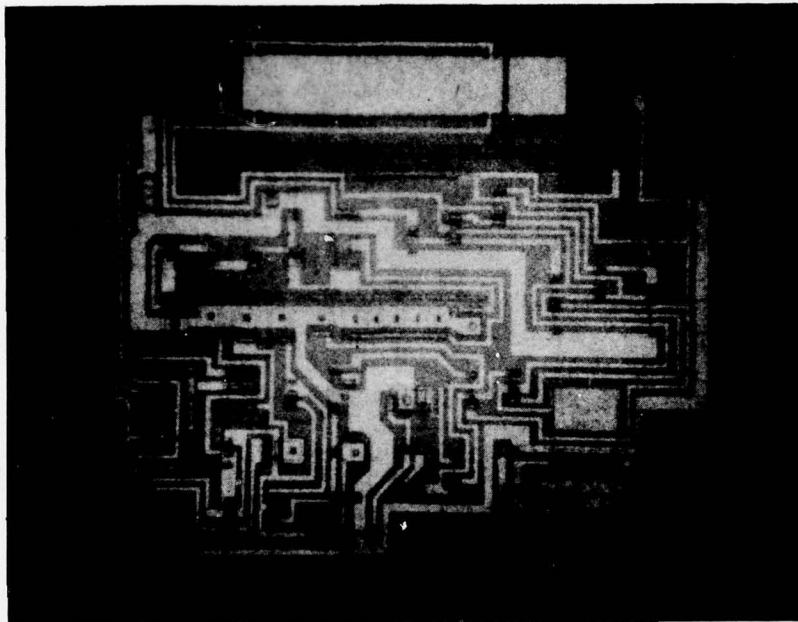


Figure 10. Phase II monolithic amplifier.

3.3.1 Parts

The TAB HMO consists of a monolithic amplifier, a substrate with three Tetrinox™ film resistors and thick film conductors, four ceramic capacitors, and three terminals.

3.3.2 Monolithic Amplifiers

The monolithic amplifiers were procured in 7.62-cm (3-inch) wafers. The wafers contain approximately 1300 testable dice. A yield of approximately 50 percent was realized during development. The wafers were glassivated with approximately 5×10^{-4} mm (5000Å) of silicon dioxide glass with 4 to 5 percent phosphorous doping. The glassivation is important since the wafers are exposed to additional processing steps during bumping.

3.3.3 Substrate and Film Resistors

The ceramic substrate, with the Tetrinox™ film resistors and thick film conductors deposited on it, was purchased from Caddock Inc. The ceramic substrate is 96 percent alumina. Its dimensions were $8.1 \times 19.4 \times 0.76$ mm ($0.320 \times 0.765 \times 0.03$ inch). The Tetrinox™ film resistor system is processed to be similar to conventional thick film resistor systems. However, the Tetrinox™ resistor system has superior temperature stability and long-term stability characteristics in comparison to conventional thick film resistor systems. Table II shows the temperature coefficient of resistance (TCR) measurements on 10 substrates. The electrical data show that the resistor TCR's are typically 8 to 15 ppm/°C.

The Tetrinox™ resistor system is terminated with a low-fire silver thick film from DuPont (Ag 7713). The thick film conductors were platinum and silver thick film conductors from DuPont (PtAg 9770). The substrate layout used for the oscillator hybrid circuit is shown in drawing 11711674, appendix A.

3.3.4 Ceramic Chip Capacitors

NPO* ceramic chip capacitors were used in the twin-T network because they exhibit superior time and temperature stability characteristics. The NPO capacitor can be procured from many suppliers with a temperature coefficient of capacitance of ± 30 ppm/°C. Ceramic capacitors are very compatible with hybrid microcircuit processing used to fabricate the TAB HMO. Ceramic capacitors with palladium and silver terminations were selected due to their compatibility with solder reflow processes and low cost.

3.3.5 Processes

Bumping — The bumping process requires an intermediate metallization layer topped with an electroplated gold bump. The intermediate or barrier metallization consists of titanium, palladium, and gold which are sputtered on the wafer. The intermediate metallization is required to provide a diffusion barrier between the aluminum bonding pad on the wafer and the electroplated gold bumps. The available aluminum bonding pads [opening in glassivation over a 0.127-mm

*NPO is an EIA code for capacitor temperature characteristic meaning "Negative-Positive-Zero."

TABLE II. TEMPERATURE COEFFICIENT OF RESISTANCE DATA

Serial No.	TCR			TCR			TCR			TCR			TCR			R at -50°C (ohm)
	R at +25°C (ohm)	25 to 45°C (ppm/°C)	R at +45°C (ohm)	R at +71°C (ohm)	R at +25°C (ohm)	25 to 0°C (ppm/°C)	R at 25 to 0°C (ohm)	R at 30°C (ohm)	25 to 30°C (ppm/°C)	R at -30°C (ohm)	25 to -50°C (ppm/°C)					
#1	R1	33,892.5	4.3	33,895.4	33,900.9	33,894.0	4.8	33,889.7	5.1	33,884.3	5.1	33,881.0				
	R2	33,886.1	13.6	33,895.3	33,904.5	22,889.5	9.9	33,880.6	10.7	33,869.2	10.8	33,861.8				
	R3	13,088.7	13.4	13,092.2	13,096.5	13,090.3	10.4	13,086.7	11.1	13,082.2	11.2	13,079.2				
#2	R1	33,840.4	7.9	33,845.8	33,851.5	33,843.3	6.1	33,837.8	6.4	33,831.2	6.2	33,827.5				
	R2	33,816.9	12.3	33,825.2	33,834.5	33,830.0	10.3	33,810.8	11.2	33,798.8	11.2	33,791.3				
	R3	13,147.3	10.6	13,150.1	13,153.5	13,146.2	11.8	13,142.1	12.5	13,137.0	12.6	13,133.4				
#3	R1	33,831.8	11.4	33,839.5	33,849.5	33,833.1	9.8	33,824.3	10.8	33,812.7	10.7	33,805.8				
	R2	33,870.6	11.4	33,878.3	33,889.2	33,870.1	12.0	33,859.3	12.9	33,845.7	12.7	33,837.4				
	R3	13,143.8	14.1	13,147.5	13,153.5	13,144.1	14.9	13,138.9	17.0	13,131.6	16.8	13,127.4				
#4	R1	33,744.4	15.4	33,754.8	33,764.6	33,746.5	11.9	33,735.8	13.0	33,722.0	13.0	33,713.5				
	R2	33,862.8	18.9	33,875.6	33,889.3	33,864.5	15.8	33,850.3	17.1	33,832.2	17.0	33,820.9				
	R3	13,104.0	21.0	13,109.5	13,116.0	13,105.6	18.7	13,099.1	20.1	13,090.0	19.9	13,085.8				
#5	R1	33,970.7	4.9	33,974.0	33,978.2	33,970.3	5.0	33,965.8	5.2	33,960.4	5.0	33,957.4				
	R2	33,934.7	10.0	33,941.2	33,950.7	33,934.2	10.5	33,924.8	11.3	33,912.7	11.3	33,905.2				
	R3	13,167.5	15.6	13,171.6	13,177.3	13,167.2	14.9	13,162.0	16.6	13,155.0	16.6	13,150.7				
#6	R1	33,909.1	11.7	33,917.0	33,928.0	33,910.6	11.0	33,900.7	11.9	33,888.1	11.8	33,880.3				
	R2	33,840.0	16.1	33,850.9	33,864.0	33,845.0	12.6	33,833.7	13.5	33,819.4	13.5	33,810.5				
	R3	13,137.0	20.4	13,132.1	13,139.3	13,127.2	19.0	13,120.6	20.9	13,111.9	20.8	13,106.5				
#7	R1	33,829.8	7.6	33,835.2	33,841.7	33,830.9	6.7	33,825.0	7.3	33,817.1	7.1	33,812.7				
	R2	33,823.2	11.9	33,833.9	33,841.8	33,827.5	9.8	33,818.7	10.1	33,808.3	10.0	33,802.0				
	R3	13,109.2	13.7	13,112.8	13,117.0	13,108.6	14.1	13,103.7	15.2	13,097.5	15.1	13,093.6				
#8	R1	33,842.3	6.8	33,846.9	33,853.5	33,842.3	7.0	33,167.8	7.3	33,828.6	6.9	33,824.5				
	R2	33,883.2	10.6	33,890.4	33,900.0	33,883.4	10.1	33,874.3	11.0	33,862.5	10.8	33,855.7				
	R3	13,172.7	14.4	13,176.5	13,182.0	13,172.8	14.3	13,167.8	15.2	13,161.6	15.3	13,157.5				
#9	R1	33,903.9	7.7	33,909.1	33,915.1	33,904.3	6.9	33,878.1	7.3	33,890.5	7.1	33,886.0				
	R2	33,873.1	10.6	33,880.3	33,872.3	33,866.3	11.1	33,851.2	11.1	33,831.6	10.8	33,844.5				
	R3	13,109.4	19.8	13,114.6	13,122.4	13,111.6	18.1	13,105.3	19.5	13,097.3	19.3	13,092.4				
#10	R1	33,875.5	5.0	33,878.9	33,880.5	33,876.7	2.6	33,874.4	2.6	33,871.8	2.3	33,870.8				
	R2	33,920.8	9.6	33,927.3	33,932.9	33,924.0	6.3	33,918.3	6.9	33,911.0	6.6	33,907.1				
	R3	13,098.1	6.5	13,100.8	13,104.5	13,094.7	9.8	13,094.7	10.5	13,090.0	10.4	13,087.4				

Δ T = 20 Δ T = 46 Δ T = 26.5 Δ T = 55.9 Δ T = 75.7

Δ T = 75.7

Δ T = 55.9

Δ T = 26.5

Δ T = 46

Δ T = 20

(5-mil) square aluminum bonding pad] on the monolithic amplifier die are 0.12-mm (4.6-mil) squares. There are eight bonding pads per die. The gold bump extends approximately 0.005 mm (0.2 mil) past the edge of the window in the glassivation. It is important that the gold bump not extend past the edge of the aluminum bonding pad below to prevent microfracturing. The gold bumps are electroplated to a height of approximately 0.025 mm (1 mil). Figure 11 shows the gold bumps on a monolithic amplifier.

Tape Automated Bonding (TAB) — The tape format consists of 35-mm Kapton with adhesively bonded rolled annealed copper (three layers). Carrier frames consist of 1-oz rolled annealed copper laminated to 0.127-mm (5-mil) thick Kapton tape. The copper leads are $3.56 \times 10^{-2} \pm 0.0051$ mm (1.4 ± 0.2 mil) thick. The copper lead frames are tin plated (tin plate thickness = 7.62×10^{-4} mm or 30 μ in. Drawings 34028099 and 34026856, appendix A, illustrate the present lead frame design. Figure 12 shows the monolithic amplifier in the tape carrier.

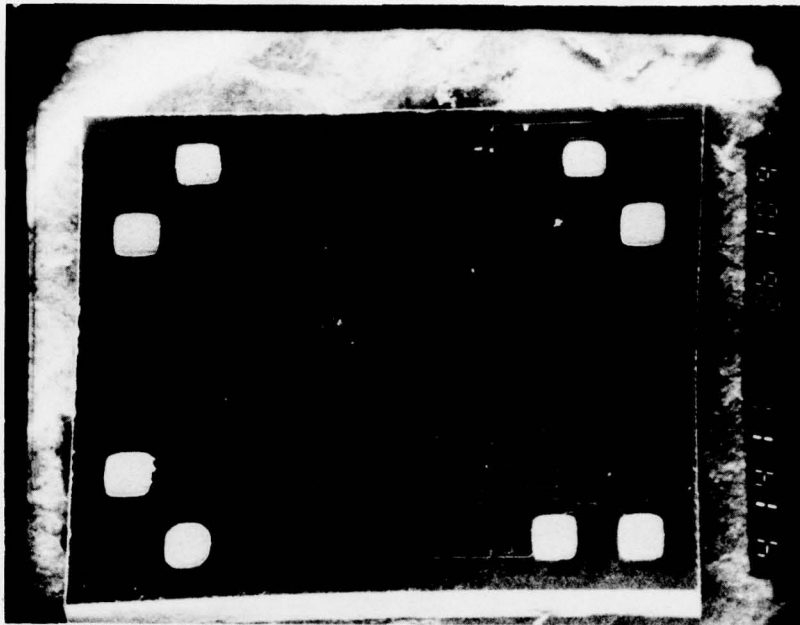
Inner Lead Bonding — The inner lead bonding process employs gang bonding. The process joins the tin-plated copper lead frames to the gold bumps on the die. Heat and pressure are applied to the tin-plated copper leads, which are placed on the gold bump, forming a gold-tin eutectic. Tests performed on the first lot of inner lead bonded monolithic amplifiers revealed pull strengths ranging from 30 to 40 and broken leads in every case. Figure 13 shows the inner lead bonds on the monolithic amplifier.

Excising and Lead Forming — The excising operation removes the inner lead bonded monolithic amplifiers and a portion of the attached lead frame from the tape carrier by severing the leads. Lead forming shapes the leads to provide sufficient clearance between the leads and the edge of the amplifier die to prevent short-circuiting. It also shapes the leads so that the designated area of the lead can be attached to the thick film outer lead bonding pad. The shape of the leads is illustrated in drawing 34028099, appendix A.

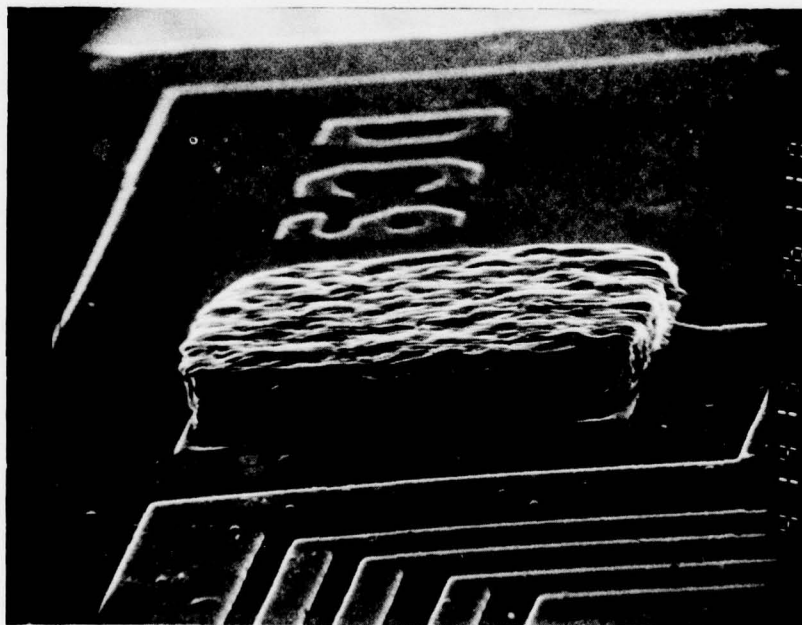
Solder Reflow — The ceramic chip capacitors, monolithic amplifier, and terminals are attached to the thick film conductors utilizing solder reflow techniques. Solder paste (62 percent tin, 36 percent lead, and 2 percent silver) was screen printed on the thick film conductor bonding pads. The reflow process was performed in a Watkins-Johnson conveyor furnace specifically designed to achieve spike profiles. This feature is desirable since excessive time above the melting point of solder degrades the adhesion of the thick-film conductors.

3.3.6 Active Trimming

The active trimming was automatically performed by utilizing a Model 25 ESI laser system. The oscillator is biased with -23.5 Vdc. The analog output of the monolithic amplifier is monitored to indicate when the proper trim point has been achieved. The analog output is fed into a buffer circuit to prevent loading from the ac voltmeter. The laser minicomputer system is programmed to trim R3 until the Vrms voltage decreases to less than 200 mVrms. After R3 has been adjusted, the laser automatically cuts open a thick film conductor which removes a short circuit across a resistor on the monolithic amplifier. This removal increases the gain of the monolithic amplifier approximately 1.5 dB, satisfying the conditions for oscillation, and the oscillator begins to run.



Bumped monolithic amplifier die.



Enlarged view of gold bump.

Figure 11. Illustration of bumping process.

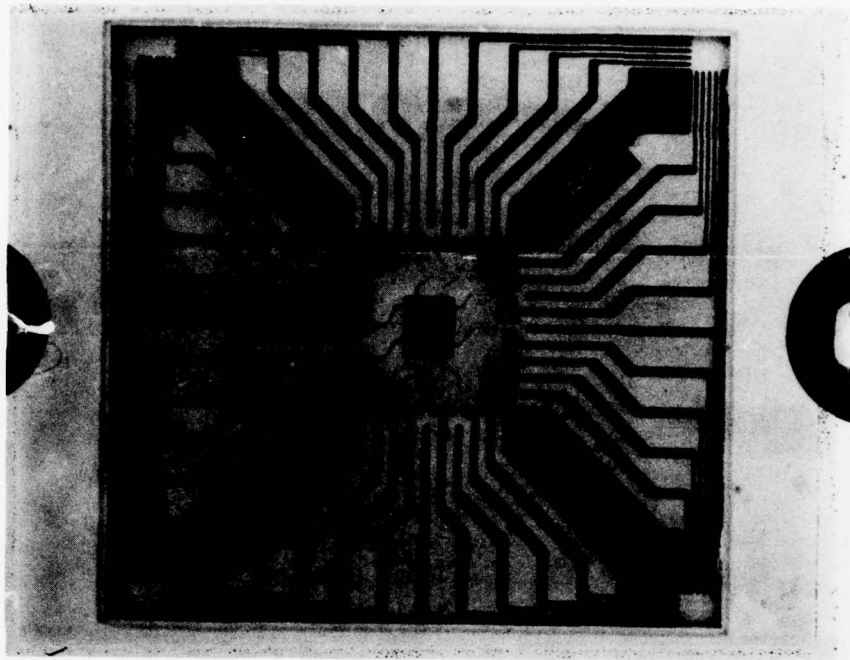


Figure 12. Monolithic amplifier in tape carrier.

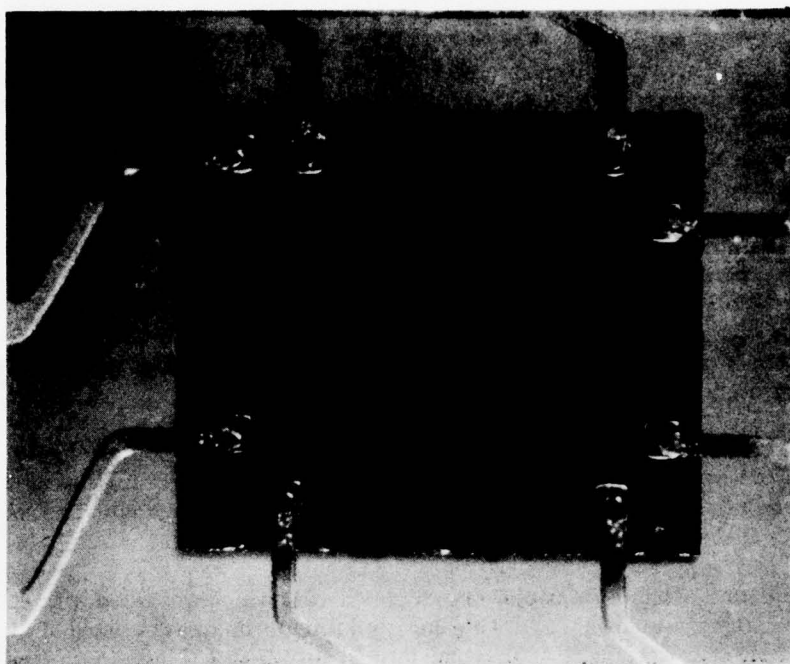


Figure 13. Inner lead bonded monolithic amplifier.

3.3.7 Fabrication and Packaging

The fabrication steps are identified in the TAB HMO process flow chart, figure 14.

The monolithic amplifier wafers were processed by utilizing TCC and TAB technology. The wafers were bumped, mounted on a substrate coated with adhesive, sawed, and inner lead bonded. Tape carrier lead frame was a 35-mm Kapton tape, which allowed the monolithic amplifiers to be handled in reel form after the inner lead bonding process. The tape chip carrier allowed electrical testing after bumping and inner lead bonding processes. The ac electrical testing had a considerable effect on increasing the yield of the hybrid microcircuit oscillator assembly. The monolithic amplifier and a portion of the tin-plated copper lead were excised from the lead frame. Lead forming was performed subsequent to excising. The lead forming operation formed the tin-plated copper leads so that contact could be made with the thick film bonding pads on the substrate without short-circuiting to the edge of the die. The tin-plated copper heads which were the interconnections from the monolithic amplifier to the thick film bonding pads were 3.5×10^{-2} mm (1.4 mil) thick and 0.076 mm (3 mil) wide at the gold bumps.

A nonconductive epoxy was used to aid in fastening the monolithic amplifier to the ceramic substrate. Solder paste was screen printed on the thick film bonding pads to form the connections to the monolithic amplifier leads, ceramic capacitor terminations, and terminals. The solder paste was reflowed in a conveyor furnace capable of delivering a spike profile.

The oscillator substrate assembly was placed in a plastic case which was filled with epoxy. Two encapsulating techniques were evaluated. One encapsulating technique consisted of dipping the substrate in silicone (Dow Corning R6100), which formed a 0.127 to 0.17-mm (5- to 7-mil) barrier layer over the components and entire substrate. Subsequent to the silicone dipping, the substrate was placed in the plastic case filled with epoxy. The other encapsulating technique consisted of placing the substrate in the plastic case without the silicone barrier layer. A metal clip was placed on the plastic case, and the case was dipped in a conductive paint to form a shield. A metal case is being designed for future use since it is felt that the conductive paint does not offer a satisfactory shield for this application.

3.4 ELECTRICAL AND ENVIRONMENTAL TESTING OF PROTOTYPE TAB HMOs

Prototype TAB HMOs were fabricated as described in section 3.3 by using the Phase I monolithic amplifier design. Group 1 (SN1-14) devices were encapsulated by using epoxy, whereas group 2 (SN15-28) devices were encapsulating by using a silicone barrier layer and epoxy. Twenty-seven TAB HMOs were exposed to electrical and environmental testing per drawing 11726813 as shown in figure 15 (see appendix A). Group A electrical data are contained in table IV. The temperature coefficients of the period (TCT) are summarized in table III.

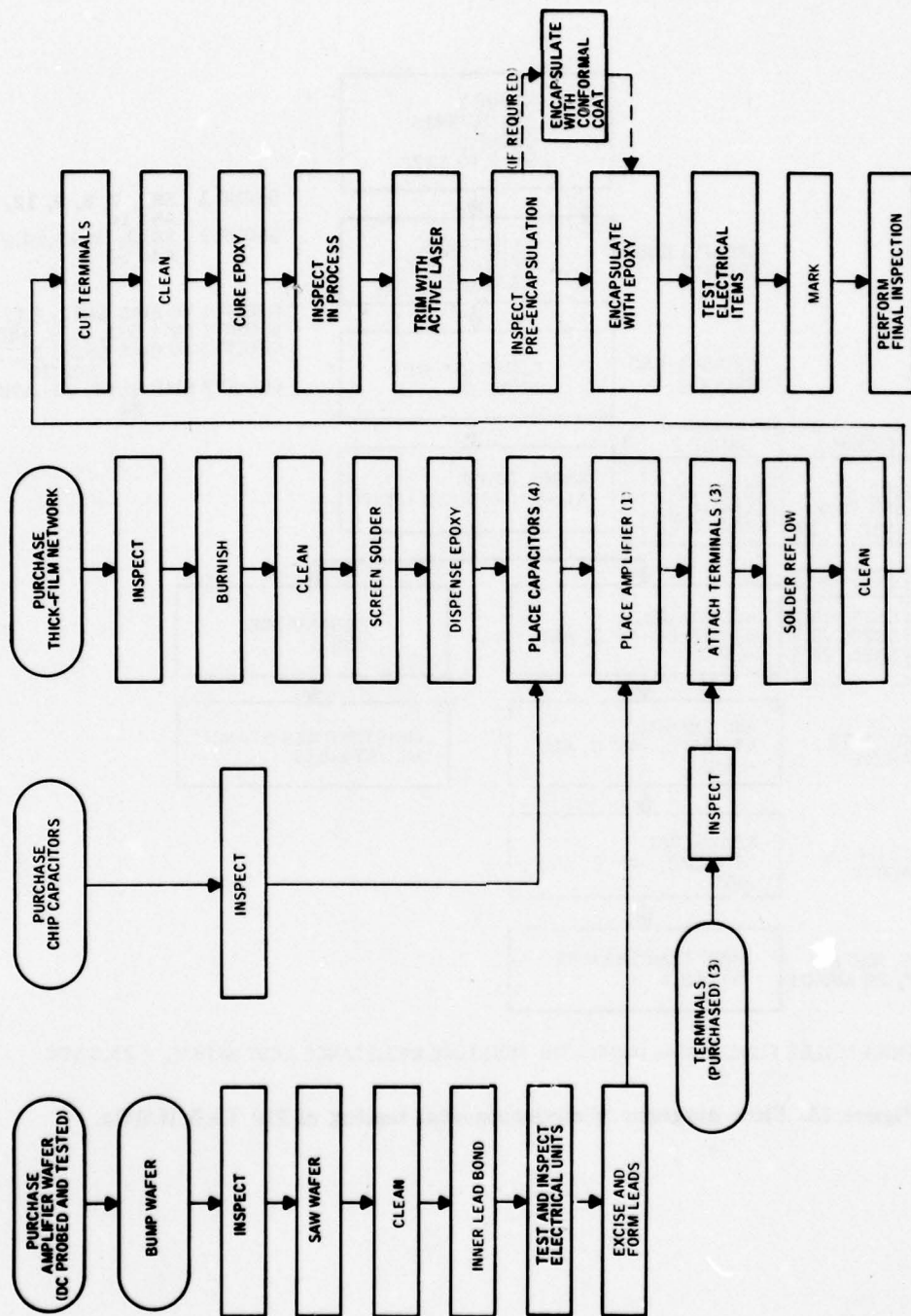
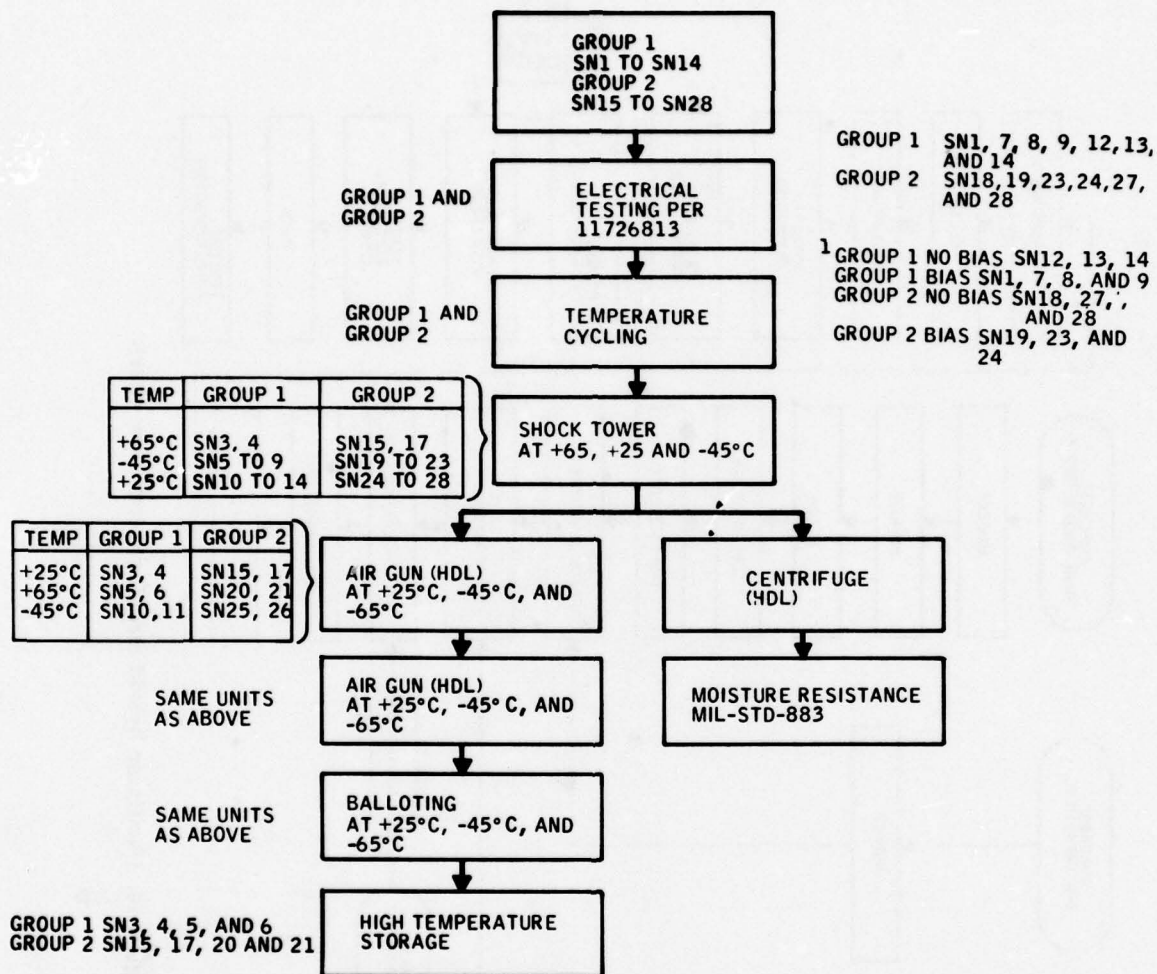


Figure 14. Oscillator hybrid circuit process flow chart.



¹ SEVEN BIASED DEVICES WERE FUNCTIONING DURING THE MOISTURE RESISTANCE TEST WITH $V_S = 23.5$ VDC

Figure 15. Flow diagram of environmental testing of 210 TAB HMOs.

TABLE III. TEMPERATURE COEFFICIENT OF PERIOD

Group 1						
Temperature	(°C)	25 to 45	25 to 71	25 to 0	25 to -30	25 to -50
\bar{X} TCT	(ppm/°C)	38.0	36.2	38.0	36.0	39.8
Low TCT	(ppm/°C)	28.2	26.5	28.2	25.2	29.3
High TCT	(ppm/°C)	59.6	59.6	63.4	51.7	56.7
Group 2						
Temperature	(°C)	25 to 45	25 to 71	25 to 0	25 to -30	25 to -50
\bar{X} TCT	(ppm/°C)	15.3	12.8	18.0	19.1	21.0
Low TCT	(ppm/°C)	6.0	4.1	7.6	10.6	11.3
High TCT	(ppm/°C)	30.9	27.7	37.2	37.8	41.7

3.4.1 Temperature Cycle Test

The period drift exhibited during temperature cycling testing (+71° to -55°C) is shown in table V.

The oscillator period drift through temperature cycling did not display any deleterious affects on the oscillator performance.

3.4.2 Shock Test

The period drift exhibited during shock testing (30 kg) is shown in table VI.

Four of the TAB HMOs (SN2, 13, 16 and 24) did not function electrically after potting in the brown sugar prior to the shock testing. Devices SN2 and SN13 were drawing high current. After removal from the brown sugar, SN13 and SN24 functioned properly, whereas SN2 and SN16 did not function electrically. Failure analysis did not reveal any obvious visual defects. It appears that short circuit conditions (SN2 and SN13), open circuit conditions (SN24), and improper connections external to the hybrid microcircuit oscillator assemblies resulted in abnormal test results for these four devices.

Device SN19 exhibited a period drift of -166.4×10^{-9} . Failure analysis did not reveal any visual defects in the elements of the TAB HMO assembly. However, minor shifts in the resistance or capacitance values of the twin-T network could occur and would not be detectable because the initial component values are unknown.

3.4.3 Constant Acceleration Test

Thirteen of the prototype TAB HMOs were exposed to constant acceleration testing. The constant acceleration tests were performed by HDL. The period drift noted during the constant acceleration testing was well within the specified limits. The period drift exhibited during the constant acceleration tests is shown in table VII.

TABLE IV. GROUP A ELECTRICAL DATA ON PROTOTYPE TAB HMO

SN	T at 25°C and 23.5 Vdc (10 ⁻⁶ s)	Voltage Sensitivity			Temperature Sensitivity					Temperature Coefficient (TCr)				
		ΔT 23.5 Vdc to 17 Vdc (10 ⁻⁹ s)	ΔT 23.5 Vdc to 30 Vdc (10 ⁻⁹ s)	ΔT 25°C to 45°C (10 ⁻⁹ s)	ΔT 25°C to 71°C (10 ⁻⁹ s)	ΔT 25°C to 0°C (10 ⁻⁹ s)	ΔT 25°C to 50°C (10 ⁻⁹ s)	ΔT 25°C to 71°C (10 ⁻⁹ s)	ΔT 25°C to 50°C (10 ⁻⁹ s)	25°C to 45°C (ppm/°C)	25°C to 71°C (ppm/°C)	25°C to 0°C (ppm/°C)	25°C to -30°C (ppm/°C)	25°C (ppm/°C)
Spec Limits	96 - 107	±12	±15	±150	±350	±180	±410	±580		±75	±75	±75	±75	±75
1	99.9518	6.8	-7.8	79.1	159.9	-93.3	-212.8	-299.9		34.8	37.2	38.6	38.6	40.0
2	100.4761	9.9	-6.6	70.6	148.3	-94.2	-201.2	-268.2		32.0	37.8	36.6	36.6	35.6
3	97.9122	6.4	-7.0	64.1	136.5	-78.7	-166.7	-256.8		32.7	30.2	31.0	31.0	35.0
4	98.9644	8.4	-5.4	91.6	206.6	-112.3	-242.9	-360.6		46.5	45.5	45.3	44.6	48.6
5	98.9132	5.6	-10.1	60.8	131.6	-22.1	-189.7	-267.2		30.8	28.8	8.9	34.9	36.0
6	99.0784	7.6	-6.8	63.8	138.1	-83.7	-174.4	-290.7		32.2	30.3	33.8	32.0	39.1
7	96.8986	0.3	-15.3	77.2	176.2	-109.0	-221.2	-317.7		39.8	39.5	45.0	41.5	43.7
8	99.2690	8.2	-6.4	84.5	178.1	-105.2	-213.8	-354.3		42.6	39.0	42.4	39.2	47.6
9	99.8809	9.6	-5.9	56.7	120.8	-70.0	-137.4	-219.3		28.4	26.5	28.2	25.2	29.5
10	96.7971	9.1	-5.5	54.6	120.3	-68.6	-131.9	-212.7		28.2	27.0	28.3	24.8	29.3
11	100.7270	9.5	-5.2	78.1	178.5	-99.0	-192.5	-294.9		38.8	38.5	39.3	34.7	39.0
12	99.3864	6.7	-7.4	118.4	232.0	-157.5	-282.6	-423.0		59.6	55.1	63.4	51.7	56.7
13	102.8017	5.7	-7.7	94.5	213.0	-121.7	-214.8	-331.9		46.0	45.0	47.5	38.0	43.0
14	97.6091	6.1	-5.8	62.5	156.6	-103.4	-167.4	-252.5		32.0	34.9	42.4	31.2	34.5
15	101.7518	6.6	-7.8	12.0	12.2	-19.3	-59.6	-86.3		6.0	4.1	7.6	10.6	11.3
16	96.4845	5.4	-10.1	31.6	59.2	-48.2	-119.9	-171.4		16.4	13.3	20.0	22.6	23.7
17	96.3857	7.3	-7.1	17.3	21.7	-26.5	-70.9	-114.4		9.0	5.0	11.0	13.4	15.8
18	100.6152	6.8	-7.0	25.9	45.8	-33.1	-88.2	-118.6		12.9	9.9	13.2	15.9	15.7
19	97.4153	9.2	-6.5	57.9	122.1	-78.4	-191.2	-284.0		29.7	27.3	32.2	35.7	38.9
20	98.2824	3.4	-11.9	22.9	35.7	-34.0	-79.9	-108.4		11.7	7.9	13.8	14.8	14.7
21	98.4986	4.7	-4.8	60.8	125.4	-91.5	-205.0	-307.7		30.9	27.7	37.2	37.8	41.7
23	98.3524	9.4	-4.9	37.8	78.5	-50.9	-108.0	-145.7		19.2	17.4	20.7	20.0	19.8
24	99.7289	11.6	-4.6	26.5	48.5	-39.9	-87.7	-128.8		13.3	10.6	16.0	16.0	17.2
25	100.0990	10.1	-5.7	24.1	47.9	-33.2	-87.9	-138.5		12.0	10.4	13.3	16.0	18.4
26	98.8017	1.8	-8.7	22.5	42.8	-37.8	-76.0	-126.3		11.4	9.4	15.3	14.0	17.0
27	103.3157	7.3	-6.9	27.6	48.1	-32.2	-108.0	-108.0		13.4	10.1	12.5	12.3	13.9
28	98.0478	22.8	+143.0	25.6	47.0	-52.8	-103.0	-181.7		13.1	10.4	21.5	19.1	24.7

¹ SN 1 - 14 were encapsulated with epoxy only.

² SN 15 - 27 were encapsulated with silicone barrier layer and epoxy.

TABLE IV. GROUP A ELECTRICAL DATA ON PROTOTYPE TAB HMO (CONCLUDED)

SN	Supply Current at 23.5 Vdc		Rise Time		Fall Time		Time High		Amplitude of Square Wave Output				
	at 25°C (mAdc)	at 71°C at -50°C (mAdc) (mAdc)	at 25°C (μs)	at 71°C at -50°C (μs)	at 25°C (μs)	at 71°C at -50°C (μs)	at 25°C (μs)	at 71°C at -50°C (μs)	at 25°C (μs)	at 71°C at -50°C (μs)	V p-p	V p-p	
Spec Limits	2.7 mAdc max		3.0 μs max		3.0 μs max		35 μs min - 60 μs max						
1	1.94	1.88	1.89	0.17	0.18	0.16	0.18	0.19	0.20	47	46	12	12
2	1.99	1.93	1.96	0.17	0.18	0.16	0.18	0.18	0.20	48	47	12	12
3	1.97	1.91	1.92	0.16	0.17	0.16	0.18	0.18	0.20	46	45	12	12
4	1.94	1.88	1.93	0.16	0.18	0.16	0.19	0.20	0.20	46	44	12	12
5	1.92	1.86	1.86	0.18	0.19	0.18	0.16	0.17	0.19	48	46	12	12
6	1.92	1.86	1.87	0.17	0.19	0.16	0.18	0.19	0.20	46	44	12	12
7	1.96	1.90	1.94	0.17	0.18	0.17	0.17	0.18	0.17	46	45	12	12
8	1.96	1.91	1.89	0.16	0.16	0.15	0.22	0.22	0.25	47	44	12	12
9	1.93	1.89	1.87	0.16	0.17	0.16	0.17	0.18	0.20	47	46	12	12
10	1.95	1.89	1.91	0.16	0.18	0.16	0.18	0.19	0.20	46	45	12	12
11	1.97	1.92	1.93	0.16	0.17	0.16	0.19	0.19	0.20	48	47	12	12
12	1.84	1.79	1.81	0.16	0.17	0.15	0.18	0.19	0.20	46	44.5	12	12
13	1.99	1.92	1.99	0.16	0.17	0.15	0.15	0.16	0.16	48	47	12	12
14	5.41	4.77	6.41	0.17	0.18	0.16	0.17	0.19	0.18	46	44.5	12	12
15	1.93	1.89	1.86	0.17	0.18	0.17	0.18	0.18	0.20	48	47	12	12
16	1.93	1.89	1.84	0.18	0.19	0.18	0.16	0.15	0.17	46	45	12	12
17	1.95	1.91	1.87	0.16	0.17	0.16	0.17	0.17	0.20	45	45	12	12
18	1.94	1.90	1.89	0.16	0.17	0.16	0.18	0.18	0.20	47	46	12	12
19	1.94	1.90	1.86	0.17	0.18	0.16	0.18	0.18	0.20	46	45	12	12
20	1.93	1.90	1.87	0.16	0.17	0.16	0.19	0.19	0.20	46	46	12	12
21	2.04	2.00	2.01	0.15	0.16	0.15	0.18	0.18	0.20	46	46	12	12
23	1.94	1.91	1.88	0.17	0.16	0.15	0.24	0.25	0.27	47	46	12	12
24	2.02	1.98	1.95	0.16	0.17	0.16	0.16	0.18	0.18	48	47	12	12
25	1.93	1.90	1.84	0.16	0.17	0.17	0.19	0.19	0.22	48	47	12	12
26	2.02	1.97	1.96	0.15	0.17	0.15	0.20	0.20	0.23	47	46	12	12
27	1.95	1.92	1.90	0.16	0.17	0.16	0.18	0.18	0.19	48	47	12	12
28	5.15	4.25	6.60	0.15	0.16	0.15	0.22	0.23	0.24	46	46	12	12

TABLE V. PERIOD DRIFTS DURING TEMPERATURE CYCLING

SN	ΔT (10^{-9} s)	SN	ΔT (10^{-9} s)
1	2.3	15	1.4
2	-17.3	16	0
3	-5.2	17	-1.0
4	-2.4	18	-1.0
5	-11.3	19	3.7
6	-11.1	20	0.3
7	-10.2	21	-1.5
8	-1.9	23	-1.6
9	-6.3	24	-22.7
10	-8.9	25	2.1
11	-13.8	26	-2.0
12	-9.0	27	-2.6
13	-3.9	28	1.3
14	6.6		
\bar{X}	-4.6		-1.82
σ	8.06		6.53
Spec Limit	± 250		± 250

TABLE VI. PERIOD DRIFTS DURING SHOCK TESTING (30 kg)

SN	ΔT (10^{-9} s)	SN	ΔT (10^{-9} s)
1	-9.2	15	0
2	—	16	—
3	-6.0	17	0.5
4	-10.4	18	-0.5
5	-3.6	19	-166.4
6	-4.5	20	-1.6
7	-6.8	21	-4.5
8	-6.0	23	-2.5
9	-6.6	24	—
10	-5.8	25	-2.0
11	-4.5	26	0.7
12	4.5	27	-4.1
13	—	28	-0.7
14	-7.3		
\bar{X}	-5.5	(\bar{X} excludes SN19)	-1.47
σ	3.69		1.82
Spec Limit	± 20		± 20

TABLE VII. PERIOD DRIFTS DURING CONSTANT ACCELERATION TESTS



SN	ΔT Pre 350 RPS (10^{-9} s)	ΔT Pre-Post (10^{-9} s)	ΔT Pre 350 RPS (10^{-9} s)	ΔT Pre-Post (10^{-9} s)
Spec Limit	± 50.0	± 50	± 50	± 50.0
1	-6.9	4.7	-2.7	3.5
7	-5.8	3.6	-7.3	2.0
8	-6.6	3.5	-4.8	4.6
9	-0.9	3.7	-2.6	0.9
12	-9.0	5.5	1.5	12.5
13	-4.0	7.5	-3.2	8.9
14	-2.4	9.8	-3.1	9.2
\bar{x}	-4.6	5.5	-3.2	5.9
σ	3.32	2.38	2.65	4.30
18	-1.0	1.3	0.5	3.4
19	-1.8	2.7	-1.0	3.0
23	-1.4	3.3	2.2	3.4
24	1.0	1.5	-1.1	0.3
27	-4.3	1.0	-1.3	2.9
28	-2.6	3.1	1.0	3.4
\bar{x}	-1.7	2.2	0.05	2.7
σ	1.76	0.99	1.41	1.21

3.4.4 Moisture Resistance Test

Thirteen prototype TAB HMOs were exposed to moisture resistance testing per MIL-STD-883, Method 1004.1. Moisture resistance testing is not a requirement of drawing 11716813. However, it is an excellent test to check chemical compatibility of the materials used in fabricating the TAB HMO. Devices SN1, 7, 8, 9, 19, 23 and 24 were electrically functioning during moisture resistance exposure. The period drift noted during the moisture resistance tests is shown in table VIII.

Eleven of 13 TAB HMOs exhibited minor drifts during the moisture resistance testing. Device SN12 did not function properly after the moisture resistance exposure. Reducing the power supply voltage from -23.5 to -6.0 Vdc allowed the oscillator to function. The gain of the monolithic amplifier is higher at lower supply voltage. This type of failure mode is indicative of the twin-T network attenuation exceeding the amplifier gain (R3 drifting to a higher value). Device SN19 exhibited an abnormal period drift. Failure analysis did not reveal any visual defects. It appears that a minor shift in the resistance or capacitance values of the twin-T network caused the abnormal period drift.

3.4.5 Air Gun Test

Twelve TAB HMOs were exposed to two air gun tests by HDL. The period drift through shock testing is summarized in table IX.

TABLE VIII. PERIOD DRIFTS DURING MOISTURE RESISTANCE TESTS

SN	ΔT (10^{-9} s)	SN	ΔT (10^{-9} s)
1	36.2	18	63.3
7	38.1	19	-414.8
8	27.5	23	30.5
9	46.5	24	37.9
12	—	27	28.7
13	33.4	28	58.0
14	36.4		
\bar{X}	36.4	\bar{X} excludes SN19)	43.7
σ	6.22		15.98

TABLE IX. PERIOD DRIFTS THROUGH SHOCK TESTING

SN	First Shock (kg)	ΔT (10^{-9} s)	Second Shock (kg)	ΔT (10^{-9} s)
3	31.2	-5.6	27.5	-2.3
4	31.2	-2.0	27.5	-3.8
5	30.9	-3.5	28.9	-7.3
6	30.9	-2.7	28.9	-2.8
10	29.9	-8.3	25.1	-11.4
11	29.9	-8.7	25.1	-39.8
\overline{X}		-5.1		-11.2
σ		2.88		14.41
15	31.2	-3.4	27.5	-1.6
17	31.2	-3.4	27.5	0.1
20	30.9	2.5	28.9	-1.5
21	30.9	-2.1	28.9	1.1
25	29.9	0.2	25.1	-0.1
26	29.9	-2.5	25.1	—
\overline{X}		-1.5		-0.36
σ		2.76		1.16

All of the TAB HMOs met the $\pm 20 \times 10^{-9}$ s period drift specification through the first shock test. However, after the second shock test, device SN11 exhibited a period drift of -39.8×10^{-9} and SN26 did not function properly. Device SN11 was not analyzed. Device SN26 functioned electrically with the supply voltage reduced from -23.5 to -13 Vdc. Failure analysis of device SN26 did not reveal any visual defects. It appears that the resistance of R3 increased; as a result, the twin-T network attenuation exceeded the gain of the monolithic amplifier.

3.4.6 Balloting Test

Eight TAB HMOs were exposed to balloting tests by HDL. Minor period changes were noted during the balloting tests. Period drifts are summarized in table X.

3.4.7 High Temperature Storage Test

Eight TAB HMOs were exposed to high temperature storage testing ($+125^{\circ}\text{C}$) by HDL. The period drifts are summarized in table XI.

Failure analysis was performed on all devices with the exception of SN260, which was potted in a tube for 57-mm testing. Failure analysis results are documented in appendix C. Additional electrical testing of the monolithic amplifier at $V_s = -17.0$ and -30 Vdc will aid in eliminating the voltage sensitivity problem noted in devices SN5, 83, 227, and 260.

3.5 FABRICATION, ELECTRICAL TESTING, AND ENVIRONMENTAL TESTING OF FIRST ARTICLE TEST SAMPLE UTILIZING PHASE I MONOLITHIC AMPLIFIER DESIGN

Two hundred ten TAB HMOs were fabricated by the processes in section 3.3. This group used the Phase I monolithic amplifiers which were not electrically tested at the wafer level. The monolithic amplifiers were tested after inner lead bonding at the tape level using a supply voltage of -23.5 Vdc. The 210 TAB HMOs were encapsulated by using two different techniques. One hundred five were encapsulated with a silicone barrier layer 0.127 to 0.25 mm (5 to 10 mil) thick over the entire substrate. The barrier layer is applied by dipping the hybrid microcircuit substrate assembly in a small tank of R6100 silicone. The curing cycle required 1 hr at room temperature and 2 hr at 93°C . Subsequent to the curing process, the silicone coated oscillator substrate assemblies were placed in a plastic case filled with epoxy. One hundred five devices were encapsulated without the silicone barrier layer.

The 210 TAB HMOs were exposed to group A, B, and C testing of HDL drawing 11726813. The flow diagram in figure 16 shows the tests performed, sequence of testing, and sample size submitted to each test.

Group A electrical test results revealed that the TAB HMO performed well within the specification requirements. The temperature coefficient of the period characteristics are displayed on histograms in appendix B. The oscillators with the silicone barrier layer exhibited a TCT of 25 to 35 ppm/ $^{\circ}\text{C}$. The supply currents were typically 2.0 mA dc. Rise and fall times ranged from 200×10^{-9} to 400×10^{-9} s across the temperature range from $+71^{\circ}$ to -50°C . The time high was typically 48×10^{-6} to 52×10^{-6} s across the temperature range from $+71^{\circ}$ to -50°C . The period change noted during the voltage sensitivity tests typically ranged from 5×10^{-9} to 12×10^{-9} s.

TABLE X. PERIOD DRIFTS DURING BALLOTING TESTS

SN	ΔT (10^{-9} s)	SN	ΔT (10^{-9} s)
3	4.9	15	4.4
4	8.2	17	3.6
5	2.4	20	10.6
6	5.9	21	5.9
\overline{X}	5.4		5.9
σ	2.40		3.18

TABLE XI. PERIOD DRIFTS DURING HIGH TEMPERATURE STORAGE

SN	ΔT (10^{-9} s)	SN	ΔT (10^{-9} s)
Spec Limit	± 250		± 250
3	-20.7	15	-861.0
4	32.5	17	—
5	133.9	20	-89.9
6	-50.1	21	-44.0

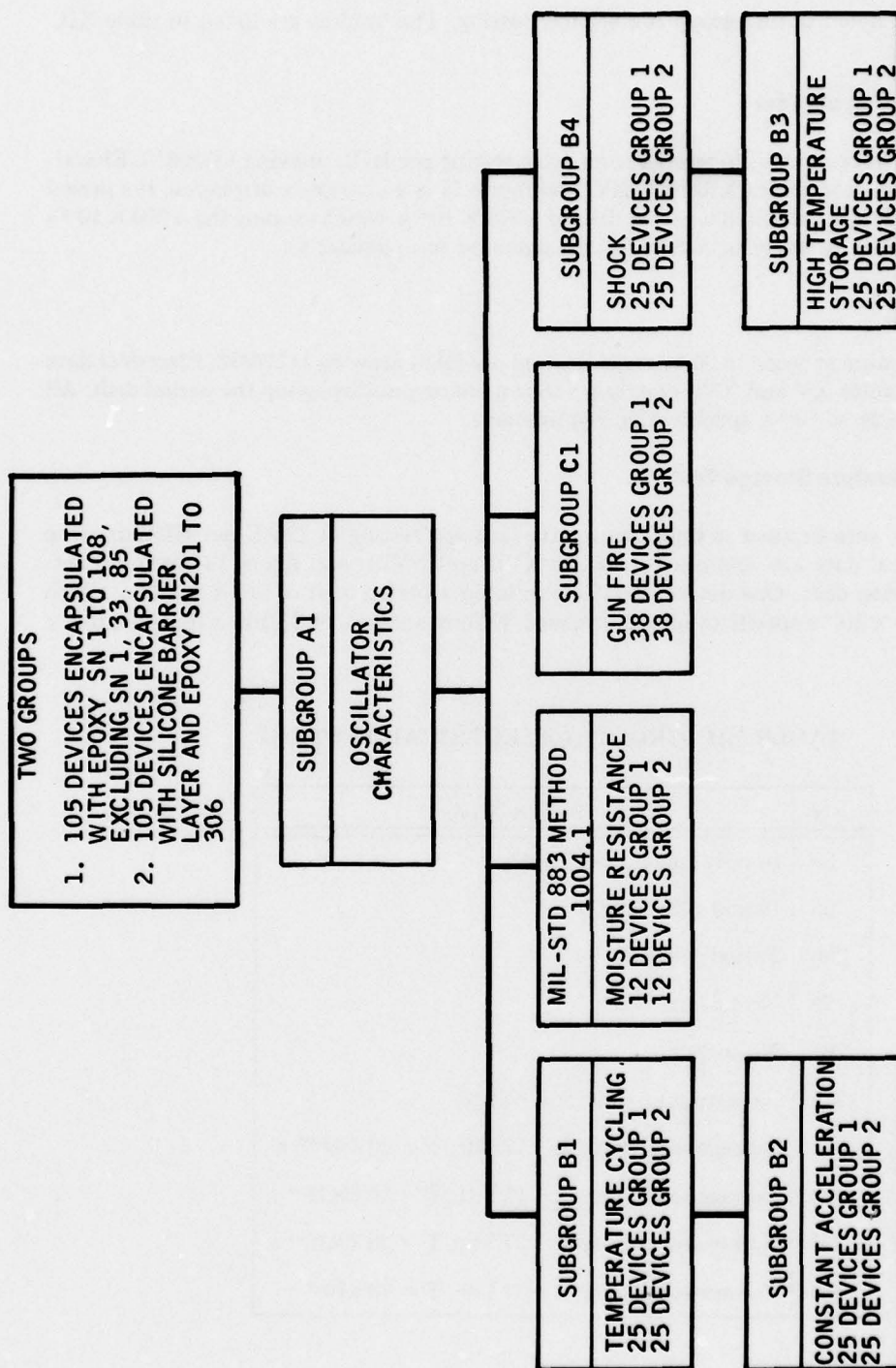


Figure 16. Flow diagram of electrical and environmental testing of 210 TAB HMOs.

Nine failures were noted during group A electrical testing. The failures are listed in table XII.

3.5.1 Temperature Cycle Test

Fifty TAB HMOs were exposed to temperature cycle testing per HDL drawing 11726813. Electrical data are contained in tables XIII and XIV, and figure 17 is a histogram displaying the period drift. One device, SN18, exhibited a period drift of -279×10^{-9} s, which exceeds the $\pm 250 \times 10^{-9}$ s maximum limit. Failure analysis of SN18 is documented in appendix C.

3.5.2 Shock Test

Fifty TAB HMOs were exposed to 30-kg shock testing per HDL drawing 11726813. Electrical data are contained in tables XV and XVI, and figure 18 is a histogram displaying the period drift. All devices met the $\pm 20 \times 10^{-9}$ s specification requirement.

3.5.3 High Temperature Storage Test

Fifty TAB HMOs were exposed to high temperature storage testing at 125°C per HDL drawing 11726813. Electrical data are contained in tables XVII and XVIII, and figure 19 is a histogram displaying the period drift. One device, SN103, exhibited a period drift of 619.5×10^{-9} s, which exceeds the $\pm 250 \times 10^{-9}$ s specification requirement. Failure analysis of SN103 is documented in appendix C.

TABLE XII. GROUP A ELECTRICAL TESTING

SN	Failure Mode
35	Supply current > 2.7 mAdc
95	Period $< 96 \times 10^{-6}$ s
298	Period $< 96 \times 20^{-6}$ s
79	No output
294	No output
215	No output at -30° and -50°C
5	Voltage sensitivity at -17 Vdc, $T = 20 \times 10^{-9}$ s
83	Voltage sensitivity at -17 Vdc, $T = 27.5 \times 10^{-9}$ s
227	Voltage sensitivity at -17 Vdc, $T = 36.7 \times 10^{-9}$ s
260	Voltage sensitivity at -17 Vdc, $T = 79 \times 10^{-9}$ s

TABLE XIII. TEMPERATURE CYCLE TEST DATA

SN ¹	T Pretest (10 ⁻⁶ s)	T Post-test (10 ⁻⁶ s)	ΔT Pre to Post (10 ⁻⁹ s)
2	100.599	100.596	-3.0
3	99.0070	99.0040	-3.0
4	97.1072	97.0996	-7.6
5	96.2334	96.2223	-11.1
6	98.6456	98.6427	-2.9
7	100.920	100.909	-11.0
8	99.1129	99.0874	-25.5
9	100.154	100.139	-15.0
10	98.4523	98.4368	-15.5
11	98.7060	98.6982	-7.8
12	98.1528	98.1422	-10.6
13	98.4960	98.4853	-10.7
15	96.2640	96.2436	-20.4
16	96.6697	96.6594	-10.3
17	100.550	100.525	-25.0
18	97.8206	98.5416	-279.0 ²
19	97.7813	97.7613	-20.0
20	98.8406	98.8279	-12.7
21	100.658	100.629	-29.0
22	100.160	100.148	-12.0
23	98.2366	98.2193	-17.3
24	100.247	100.221	-26.0
25	96.3122	96.2844	-27.8
26	98.8172	98.8103	-6.9
			$\bar{x} = -17.10$
			$\sigma = 13.84$

¹Epoxy encapsulated only.

²The drift through temperature cycling exceeds $\pm 250 \times 10^{-9}$ s specification requirement. Not included in \bar{x} calculations.

TABLE XIV. TEMPERATURE CYCLE TEST DATA

SN ¹	T Pretest (10 ⁻⁶ s)	T Post-test (10 ⁻⁶ s)	ΔT Pre to Post (10 ⁻⁹ s)
201	98.8328	98.8318	-1.0
202	99.1788	99.1788	0
203	98.4078	98.4049	-2.9
204	100.570	100.568	-2.0
205	98.9139	98.9159	+2.0
206	97.9605	97.9585	-2.0
207	98.6009	98.5989	-2.0
208	98.3400	98.3352	-4.8
209	97.0996	97.0949	-4.7
210	98.1489	98.1460	-2.9
211	98.9247	98.9237	-1.0
212	98.2106	98.2135	+2.9
213	100.932	100.930	-2.0
214	97.8742	97.8694	-4.8
215	102.596	102.591	-5.0
216	99.2516	99.2536	+2.0
217	99.5282	99.5282	0
218	101.117	101.119	+2.0
219	99.0550	99.0501	-4.9
220	102.779	102.778	-0.1
221	99.1886	99.1886	0
222	99.2645	99.2635	-1.0
223	98.0844	98.0796	-4.8
224	99.3730	99.3730	0
225	100.190	100.184	-0.6
			$\bar{x} = -1.50$
			$\sigma = 2.42$

¹Conformal coated and epoxy encapsulated

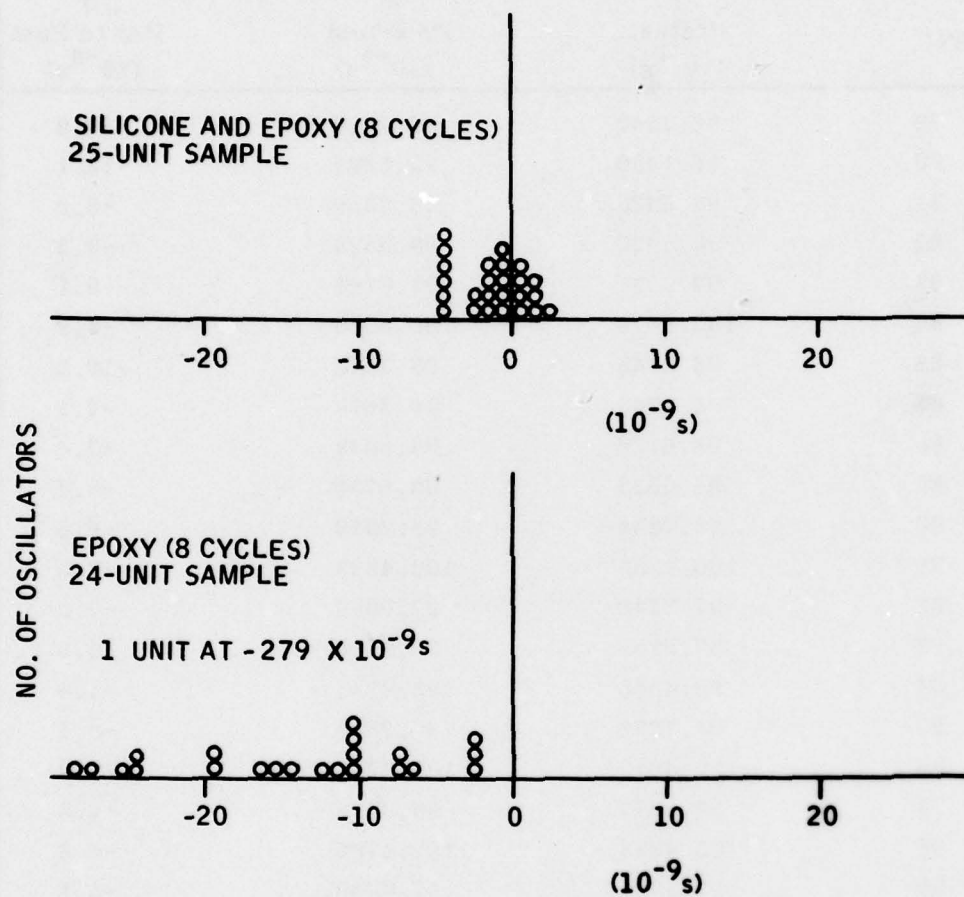


Figure 17. Histograms of period change through temperature cycling.

TABLE XV. SHOCK TEST DATA

SN ¹	T Pretest (10 ⁻⁶ s)	T Post-test (10 ⁻⁶ s)	ΔT Pre to Post (10 ⁻⁹ s)
78	96.7542	96.7462	-8.0
80	96.1450	96.1329	-12.1
81	98.6428	98.6330	-9.8
82	98.5920	98.5825	-9.5
83	97.9231	97.9140	-9.1
84	100.8614	100.8525	-8.9
86	96.8945	96.8842	-10.3
87	96.3749	96.3678	-7.1
88	98.6126	98.6048	-7.8
89	98.6823	98.6736	-8.7
90	98.2888	98.2820	-6.8
91	100.4295	100.4225	-7.0
92	97.9146	97.9076	-7.0
93	97.9256	97.9200	-5.6
94	98.4385	98.4341	-4.4
95	94.7891	94.7840	-5.1
96	100.4099	100.4040	-5.9
97	98.9077	98.9122	+4.5
98	102.4828	102.4780	-4.8
99	97.8791	97.8740	-5.1
100	97.4399	97.4350	-4.5
101	100.0499	100.0454	-4.5
102	101.0144	101.0105	-3.9
103	98.3052	98.3012	-4.0
104	97.7167	97.7131	-3.6
			$\bar{x} = -6.36$
			$\sigma = 3.23$

¹ Epoxy encapsulated only

TABLE XVI. SHOCK TEST DATA

SN ¹	T Pretest (10 ⁻⁶ s)	T Post-test (10 ⁻⁶ s)	ΔT Pre to Post (10 ⁻⁹ s)
277	98.0755	98.0750	-0.5
278	98.2163	98.2140	-2.3
279	98.1520	98.1507	-2.7
280	96.7349	96.7347	-0.2
281	96.7357	96.7330	-2.7
282	98.8199	98.8185	-1.4
283	99.0360	99.0358	-0.2
284	96.6000	96.6000	0
285	98.2467	98.2480	+1.3
286	97.9364	97.9360	-0.4
287	98.8616	98.8618	-0.2
288	100.4554	100.4560	-0.6
289	98.7535	98.7526	-0.9
290	96.6886	96.6880	-0.6
291	99.4150	99.4130	-2.0
292	98.3456	98.3449	-0.7
293	99.1864	99.1865	-0.1
295	100.2806	100.2818	+1.2
296	99.9309	99.9300	-0.9
297	97.5027	97.5017	-1.0
298	95.3325	95.3320	-0.5
299	100.3455	100.3438	-1.7
300	97.4101	97.4091	-1.0
301	98.9682	98.9674	-0.8
302	101.0681	101.0672	-0.9
		$\bar{x} = 0.79$	
		$\sigma = 0.98$	

¹Conformal coated and epoxy encapsulated.

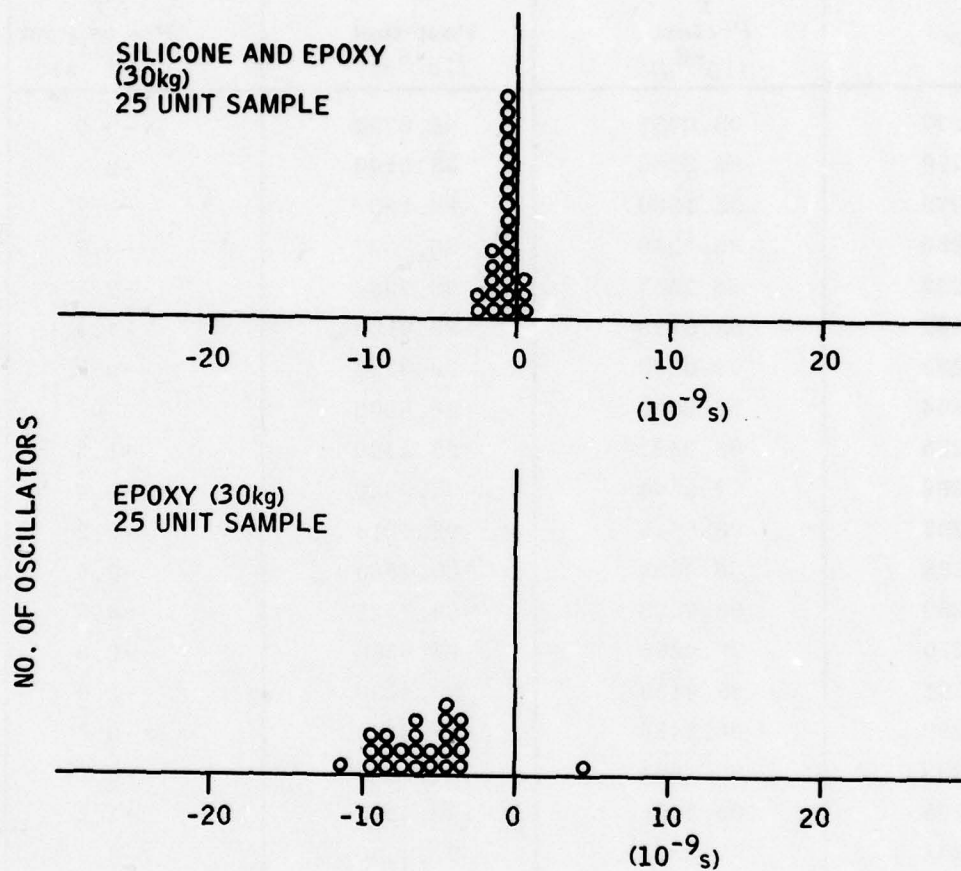


Figure 18. Histograms of period change through shock testing.

TABLE XVII. HIGH TEMPERATURE STORAGE TEST DATA

SN ¹	T Pretest (10 ⁻⁶ s)	T Post-test (10 ⁻⁶ s)	ΔT (10 ⁻⁹ s)
78	96.7780	96.7484	-29.6
80	96.1503	96.1443	-6.0
81	98.6512	98.6376	-13.6
82	98.5989	98.5984	-0.4
83	97.9320	97.9410	+9.0
84	100.8717	100.8735	+1.8
86	96.8825	96.8837	+1.2
87	96.3825	96.3764	-6.1
88	96.6100	98.6096	-0.4
89	98.6800	98.6867	+6.7
90	98.2899	98.2830	-6.9
91	100.4300	100.4190	-11.0
92	97.9172	97.9245	+7.3
93	97.9317	97.9464	+14.7
94	98.4385	98.4655	+27.0
95	94.7911	94.7899	+8.8
96	100.4120	100.4194	+7.4
97	98.9158	98.9123	-3.5
98	102.5164	102.4758	-40.6
99	97.8805	97.7880	-92.5
100	97.4403	97.4606	+20.3
101	100.0534	100.0539	+0.5
102	101.0169	101.0049	-12.0
103	98.3039	98.9234	+619.5 ²
104	97.7150	97.7224	+7.4
$\bar{x} = 4.60$			
$\sigma = 23.67$			

¹Epoxy encapsulated only

²The drift through high temperature storage exceeds the $\pm 250 \times 10^{-9}$ seconds spec limit. Not included in \bar{x} calculations

TABLE XVIII. HIGH TEMPERATURE STORAGE TEST DATA

SN ¹	T Pretest (10 ⁻⁶ s)	T Post-test (10 ⁻⁶ s)	ΔT (10 ⁻⁹ s)
277	98.0924	98.1024	+10.0
278	98.2180	98.2380	+20.0
279	98.1526	98.1827	+30.1
280	96.7370	96.7413	+4.3
281	96.7335	96.7524	+18.9
282	98.8226	98.8487	+26.1
283	99.0458	99.0570	+11.2
284	96.6022	96.6204	+18.2
285	98.2500	98.2787	+28.7
286	97.9390	97.9968	+57.8
287	98.8766	98.9031	+26.5
288	100.4573	100.4714	+14.1
289	98.7547	98.7752	+20.5
290	96.6900	96.7212	+31.2
291	99.4161	99.4410	+24.9
292	98.3496	98.3566	+7.0
293	99.1872	99.2040	+16.8
295	100.2832	100.3033	+20.1
296	99.9544	99.9617	+7.3
297	97.5086	97.5351	+26.5
298	95.3331	95.3563	+23.2
299	100.3440	100.3519	+7.9
300	97.4083	97.4270	+18.7
301	98.9667	98.9729	+6.2
302	101.0684	101.1052	+36.8
			$\bar{x} = 20.52$
			$\sigma = 11.74$

¹Conformal coated and epoxy encapsulated.

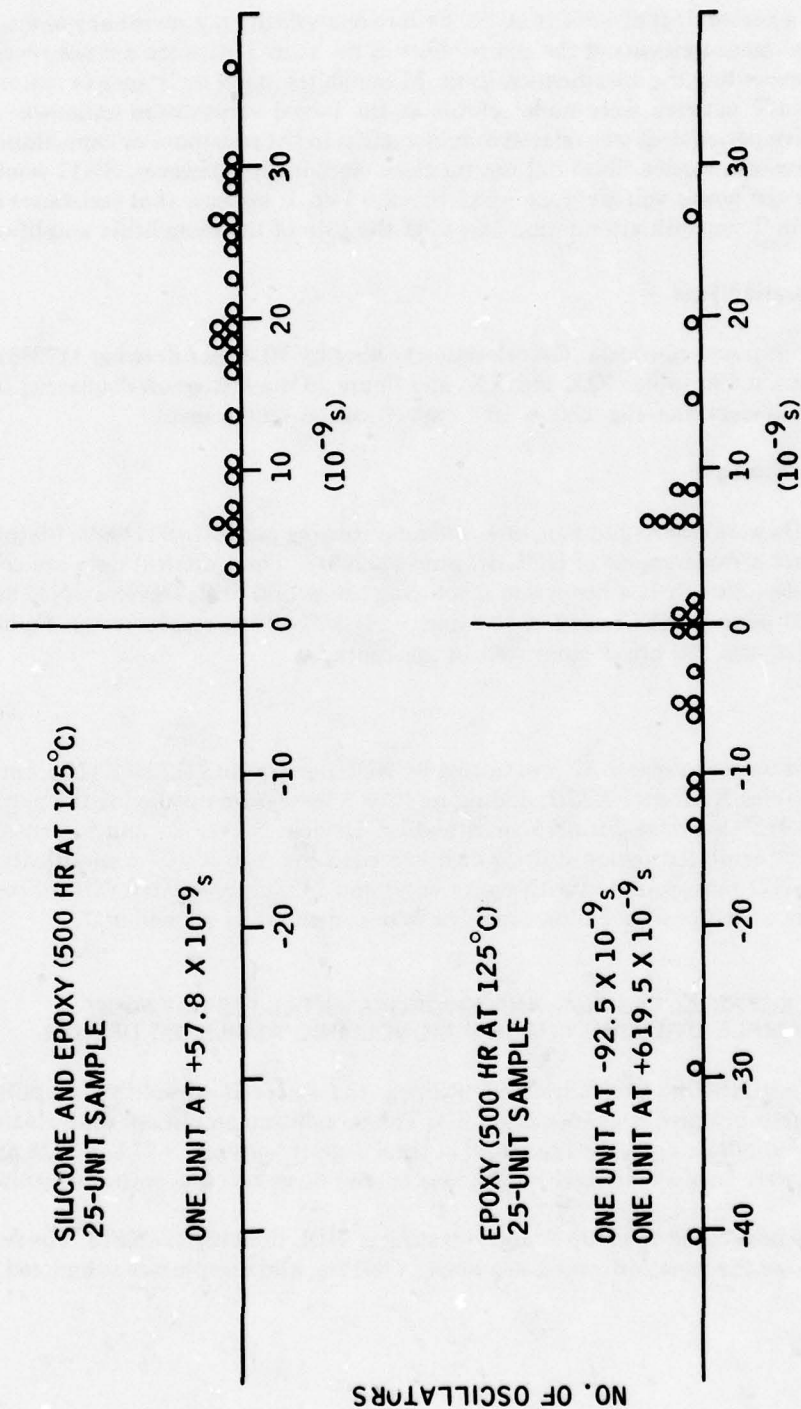


Figure 19. Histograms of period change through high temperature storage.

Device SN15 exhibited a period drift of -861×10^{-9} s. Failure analysis did not reveal any obvious visual defects. Electrical measurements of the components in the twin-T network did not reveal any component values exceeding the specification limit. Minor shifts in the resistance or capacitance values of the twin-T network were undetectable as the initial values were unknown. It appears that the excessive period drift was related to minor shifts in the resistance or capacitance values of the twin-T network. Device SN17 did not function electrically. However, SN17 would function when reducing the power voltage from -23.5 to -8.0 Vdc. It appears that resistance of R3 increased, so the twin-T network attenuation exceeded the gain of the monolithic amplifier.

3.5.4 Constant Acceleration Test

Fifty TAB HMOs were exposed to constant acceleration testing by HDL per drawing 11726813. Electrical data are contained in tables XIX and XX, and figure 20 is a histogram displaying the period drift. All of the devices met the $\pm 50 \times 10^{-9}$ s specification requirement.

3.5.5 Moisture Resistance Test

Twenty-four TAB HMOs were exposed to moisture resistance testing per MIL-STD-883, Method 1004.1. This test was not a requirement of HDL drawing 11726813. The electrical data are contained in table XXI, and figure 21 is a histogram displaying the period drift. Devices SN28 and 230 exhibited abnormal period drifts (-552×10^{-9} and -234.5×10^{-9} s, respectively). Failure analysis of devices SN28 and 230 are documented in appendix C.

3.5.6 57-mm Testing

Seventy-six TAB HMOs were exposed to 57-mm testing by HDL per drawing 11726813. Electrical data are contained in tables XXII and XXIII, and figure 22 is a histogram displaying the period drift. Five of the TAB HMOs failed during 57-mm testing. Devices SN41, 51, and 61 (encapsulated with epoxy only) exhibited period drifts which exceeded the $\pm 50 \times 10^{-9}$ s specification requirement. Devices SN71 (encapsulated with epoxy only) and 243 (encapsulated with silicone and epoxy) did not function properly. Failure analysis is documented in appendix D.

3.6 FABRICATION, ELECTRICAL TESTING, AND ENVIRONMENTAL TEST OF FIRST ARTICLE TEST SAMPLE UTILIZING PHASE II MONOLITHIC AMPLIFIER DESIGN

One-hundred-eighty TAB HMOs were fabricated utilizing the Phase II monolithic amplifier design and the manufacturing processes in section 3.3. The monolithic amplifiers were electrically tested after inner lead bonding at the tape level at three supply voltages, -23.5 , -17.0 , and -30.0 Vdc. All devices were encapsulated with a silicone barrier layer over the entire substrate.

The 180 TAB HMOs were exposed to group A and B testing of HDL drawing 11726813. The flow diagram in figure 23 shows the tests performed, sequence of testing, and sample size submitted to each test.

TABLE XIX. CONSTANT ACCELERATION TEST DATA¹

SN ²	Socket ³	T Pretest (10 ⁻⁶ s)	T 350 RPS (10 ⁻⁶ s)	T Post-test (10 ⁻⁶ s)	ΔT Pre-350 RPM (10 ⁻⁹ s)	ΔT Pre-Post (10 ⁻⁹ Test)	
201	2	98.8329	98.8330	98.8341	+0.1	+1.2	
203		98.4056	98.4097	98.4092	+4.1	+3.6	
205		98.9181	98.9168	98.9228	-1.3	+4.7	
207		98.6077	98.6097	98.6112	+2.0	+3.5	
209		97.1023	97.1024	97.1067	+0.1	+4.4	
211		98.9179	98.9252	98.9219	+7.3	+4.0	
213		100.9288	100.9355	100.9320	+6.7	+3.2	
215		102.5952	102.6035	102.5994	+8.3	+4.2	
217		99.5305	99.5330	99.5345	+2.5	+4.0	
219		99.0560	99.0552	99.0590	-0.8	+3.8	
221	2	99.1968	99.1987	99.2015	+1.9	+4.7	
223		98.0881	98.0874	98.0910	-0.7	+2.9	
225		100.1870	100.1887	100.1940	+0.3	+7.0	
202		99.1782	99.1809	99.1814	+2.7	+3.2	
204		100.5727	100.5725	100.5754	-0.2	+2.7	
206		97.9587	97.9590	97.9632	+0.3	+4.5	
208		98.3461	98.3460	98.3500	-0.1	+3.9	
210		98.1535	98.1552	98.1565	+1.7	+3.0	
212		98.1909	98.1910	98.1943	+0.1	+3.4	
214		97.8727	97.8730	97.8767	+0.3	+4.0	
216	3	99.2571	99.2576	99.2594	+0.5	+2.3	
218		101.1219	101.1225	101.1269	+0.6	+5.0	
220		102.7824	102.7843	102.7874	+1.9	+5.0	
222		99.2730	99.2747	99.2773	+1.7	+4.3	
224		99.3842	99.3858	99.3889	+1.6	+4.7	
					$\bar{x} = 3.89$		
						$\sigma = 1.11$	

¹ Tests performed by HDL.

² Conformal coated and epoxy encapsulated.

³ Orientation of hybrid oscillator in fixture.

Socket 2



Socket 3

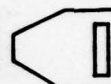


TABLE XX. CONSTANT ACCELERATION TEST DATA¹

SN ²	Socket ³	T Pretest (10 ⁻⁶ s)	T 350 RPS (10 ⁻⁶ s)	T Post-test (10 ⁻⁶ s)	ΔT Pre-350 RPM (10 ⁻⁹ s)	ΔT Pre-Post (10 ⁻⁹ s)
2	<div style="display: flex; align-items: center; justify-content: center;"><div style="margin-right: 20px;">2</div><div style="border-top: 1px solid black; width: 100%;"></div><div style="margin-left: 20px;">3</div></div>	100.5988	100.5962	100.6010	-0.6	+4.2
4		97.0972	97.0955	97.1022	-1.7	+5.0
6		98.6523	98.6514	98.6586	-0.9	+6.3
8		99.0961	99.1000	99.1050	+3.9	+8.9
10		98.4527	98.4460	98.4580	-6.7	+5.3
12		98.1540	98.1546	98.1622	+0.4	+8.2
14		98.3749	98.3775	98.3790	+2.6	+4.1
16		96.6527	96.6520	96.6588	-0.7	+6.1
18		98.5749	98.5411	98.5703	-33.8	-4.6
20		98.8421	98.8395	98.8464	-2.6	+4.3
22		98.2330	98.2345	98.2395	+1.5	+6.5
24		100.2408	100.2416	100.2470	+0.8	+6.2
3		99.0026	99.0036	99.0079	+1.0	+5.3
5		96.2260	96.2275	96.2317	+1.5	+5.7
7		100.9195	100.9190	100.9265	-0.5	+7.0
9		100.1546	100.1552	100.1613	+0.6	+6.7
11		98.7123	98.7167	98.7172	+4.4	+4.9
13		98.5005	98.5087	98.5059	+8.2	+5.4
15		96.2714	96.2731	96.2761	+1.7	+4.7
17		100.5187	100.5207	100.5244	+2.0	+5.7
18		98.5874	98.5570	98.5783	+30.4	+9.1
19		97.7625	97.7598	97.7682	-2.7	+5.7
21		100.6432	100.6485	100.6472	+5.3	+4.0
23		100.1656	100.1740	100.1700	+8.4	+4.4
25		96.3014	96.3032	96.3060	+1.8	+4.6
26		98.8278	98.8282	98.8348	+0.4	+7.0
						$\bar{x} = 5.41$

¹ Tests performed by HDL.

² Epoxy encapsulated only.

³ Orientation of hybrid oscillator in fixture.

Socket 2



Socket 3



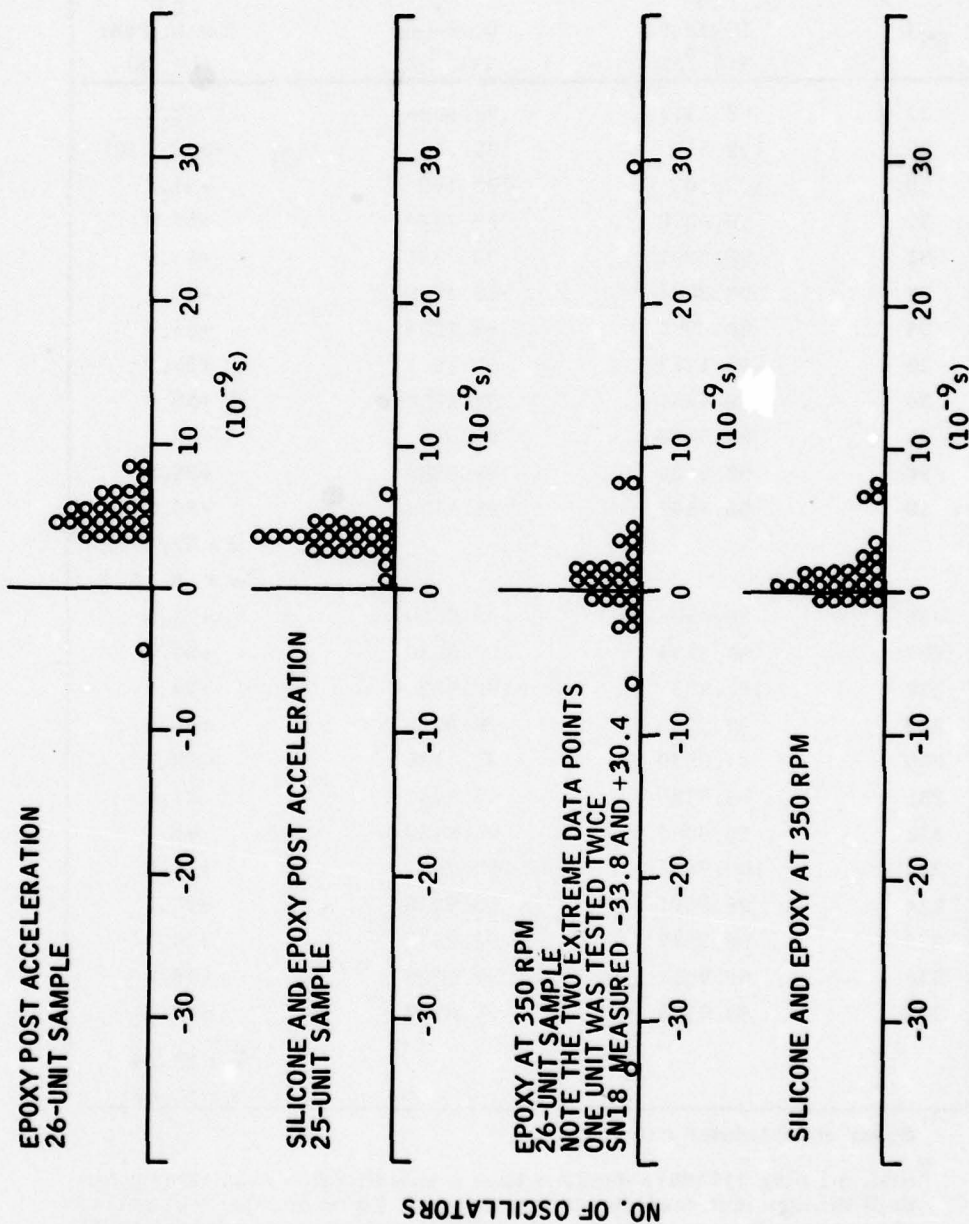


Figure 20. Histograms of period change through constant acceleration tests.

TABLE XXI. MOISTURE RESISTANCE DATA

SN ¹	T Pretest (10 ⁻⁶ s)	T Post-test (10 ⁻⁶ s)	ΔT Pre to Post (10 ⁻⁹ s)
27	98.1412	98.1836	+42.4
28	102.560	102.008	-552.0 (2)
29	103.101	103.162	+61.0
30	99.9290	99.9840	+55.0
31	96.6791	96.7361	+57.0
32	98.3894	98.4349	+45.5
34	98.6758	98.7274	+51.6
35	98.1412	98.1971	+55.9
36	96.7801	96.8354	+55.3
37	98.5096	98.5581	+48.5
38	98.9100	98.9688	+58.8
39	98.1566	98.2174	+60.8
			$\bar{x} = 53.8$
			$\sigma = 6.13$
226 ³	96.9594	96.9819	+22.5
227	98.9394	98.9630	+23.6
228	102.898	102.962	+64.0
229	97.9950	98.0315	+36.5
230	97.3530	97.1185	-234.5 ²
231	96.9725	96.9941	+21.6
232	96.6090	96.6137	+4.7
233	100.763	100.798	+35.0
234	96.5661	96.5932	+27.1
235	98.2328	98.2675	+34.7
236	96.9857	97.0020	+16.3
237	98.8123	98.8347	+22.4
			$\bar{x} = 28.04$
			$\sigma = 15.05$

¹ Epoxy encapsulated only.

² HDL drawing 11726813 does not have a specification requirement for drift through moisture resistance testing. However, the drift notes is abnormal with respect to the other devices which were exposed to this testing. Not included in \bar{x} calculations.

³ Conformal coated and epoxy encapsulated.

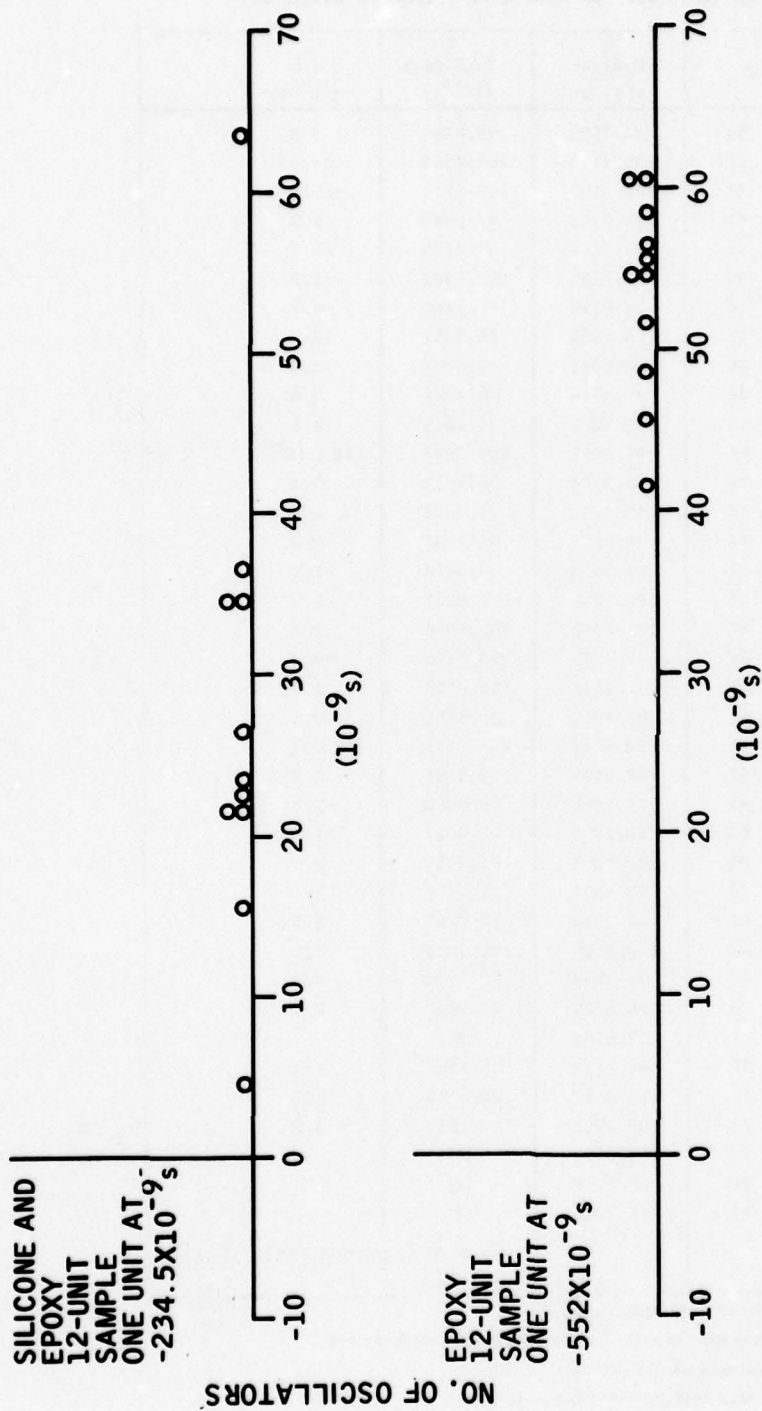


Figure 21. Histograms of period change through moisture resistance testing.

TABLE XXII. 57-mm TEST DATA TABLES

Tube No.	SN ₁	T Pretest (10 ⁻⁶ s)	T Post-test (10 ⁻⁶ s)	ΔT (10 ⁻⁹ s)
B2	40	96.8572	96.8604	3.2
	41	100.4117	100.4964	84.7 ²
B2	42	100.6090	100.5976	-11.4
	43	97.6872	97.6884	1.2
B2	44	99.2118	99.2135	1.7
B3	45	96.1355	96.1345	-1.0
	46	97.9278	97.9280	0.2
B3	47	96.9503	96.9507	0.4
	48	96.5461	96.5437	-2.4
B3	49	98.4714	98.4759	4.5
B4	50	96.3960	96.3915	-4.5
	51	98.6918	226.6093	128 x 10 ⁻⁶ ²
B4	52	98.2704	98.2777	7.3
	53	97.0522	97.0548	2.6
B4	54	96.5254	96.5245	-0.9
B5	55	98.3624	98.3614	-1.0
	56	100.3242	100.3251	0.9
B5	57	102.5099	102.5065	-3.4
	58	96.8195	96.8193	-0.2
B5	59	101.4149	101.4188	3.9
B6	60	96.7019	96.6956	-6.3
	61	96.9168	245.1698	148 x 10 ⁻⁶ ²
B6	62	97.8539	97.8565	2.6
	63	96.5915	96.5882	-3.3
B6	64	98.2037	98.2027	-1.0
B7	65	96.7654	96.7655	0.1
	66	98.6381	98.6438	5.7
B7	67	96.9218	96.9257	3.9
	68	100.3128	100.3093	-3.5
B7	69	97.7258	97.7299	4.1
B8	70	96.6022	96.6060	3.8
	71	97.6763	(3)	
B8	72	97.1253	97.1332	7.9
	73	100.5127	100.5179	5.2
B9	74	100.1799	100.1848	4.9
	75	97.2722	(4)	
B9	76	98.3246	(4)	
	77	98.1930	(4)	

$\bar{x} = 0.81$ (Excludes SN41, 51, 61)
 $\sigma = 4.18$

¹ Encapsulated with epoxy only.

² T drift exceeds 50 x 10⁻⁹ s specification requirement.

³ The output was at -12.6 Vdc.

⁴ The tube was lost during 57-mm testing.

TABLE XXIII. 57-mm TEST DATA TABLES

Tube No.	SN ¹	T Pretest (10 ⁻⁶ s)	T Post-test (10 ⁻⁶ s)	ΔT (10 ⁻⁹ s)
B2	238	97.0545	97.0575	3.0
	239	99.2567	99.2595	2.8
	240	99.3927	99.3972	4.5
	241	98.3836	98.3876	4.0
B2	242	98.1765	98.1856	9.1
B3	243	97.0255	(2)	
	244	99.8742	99.8846	10.4
	245	99.0798	99.0893	9.5
	246	102.5493	102.5528	3.5
B3	247	99.2361	99.2389	2.8
B4	248	97.9495	97.9504	0.9
	249	96.3596	96.3692	9.6
	250	100.4600	100.4598	-0.2
	251	98.4990	98.5020	3.0
B4	252	97.1961	97.1974	1.3
B5	253	98.5151	98.5205	5.4
	254	100.6174	100.6296	12.2
	255	97.0131	97.0167	3.6
	256	97.0768	97.0825	5.7
B5	257	98.1690	98.1696	0.6
B6	258	100.6110	100.6119	0.9
	259	98.1559	98.1558	-0.1
	260	98.1408	98.1398	-1.0
	261	99.2832	99.2849	1.7
B6	263	98.4077	98.4121	4.4
B7	264	102.3091	102.3156	6.5
	265	98.0567	98.0645	7.8
	266	98.3515	98.3563	4.8
	267	98.6359	98.6361	0.2
B7	268	98.8229	98.8245	1.6
B8	269	96.6696	96.6731	3.5
	270	98.0867	98.0929	6.2
	271	96.2629	96.2667	3.8
	272	100.7808	100.7824	1.6
B8	273	99.3674	99.3712	3.8
B9	274	99.1425	(3)	
	275	98.4370	(3)	
B9	276	97.9988	(3)	
				$\bar{x} = 4.04$
				$\sigma = 3.31$

1 Devices encapsulated with silicone and epoxy

2 The output was at -12.4 Vdc

3 The tube was lost during 57-mm testing

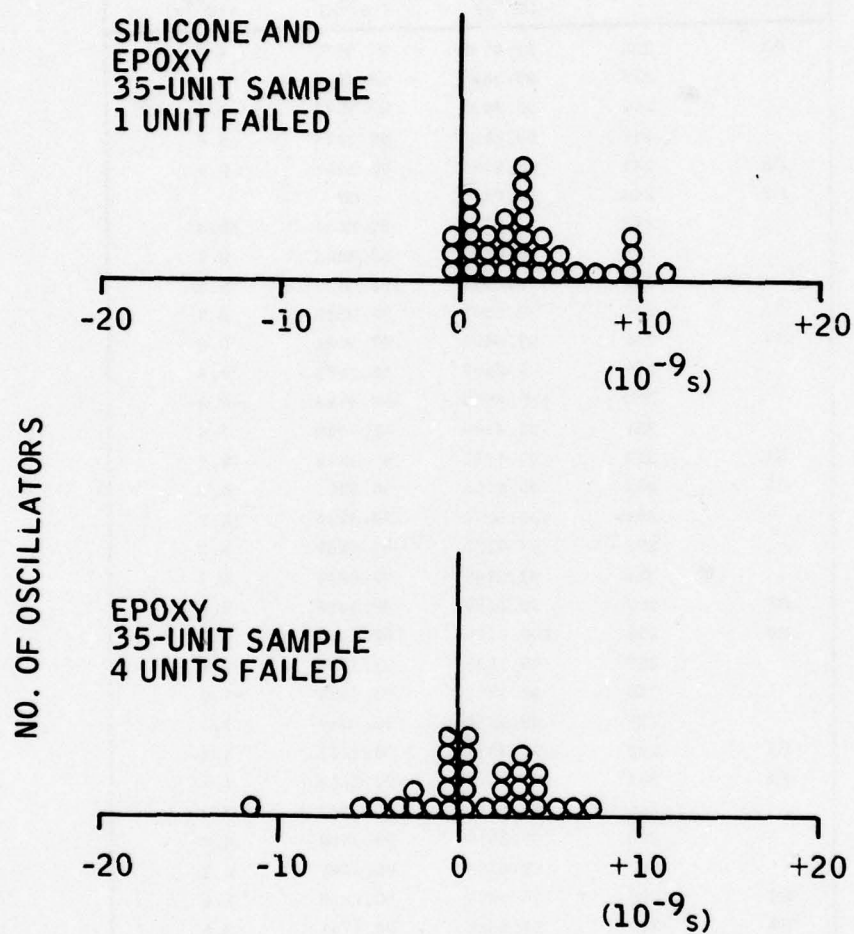
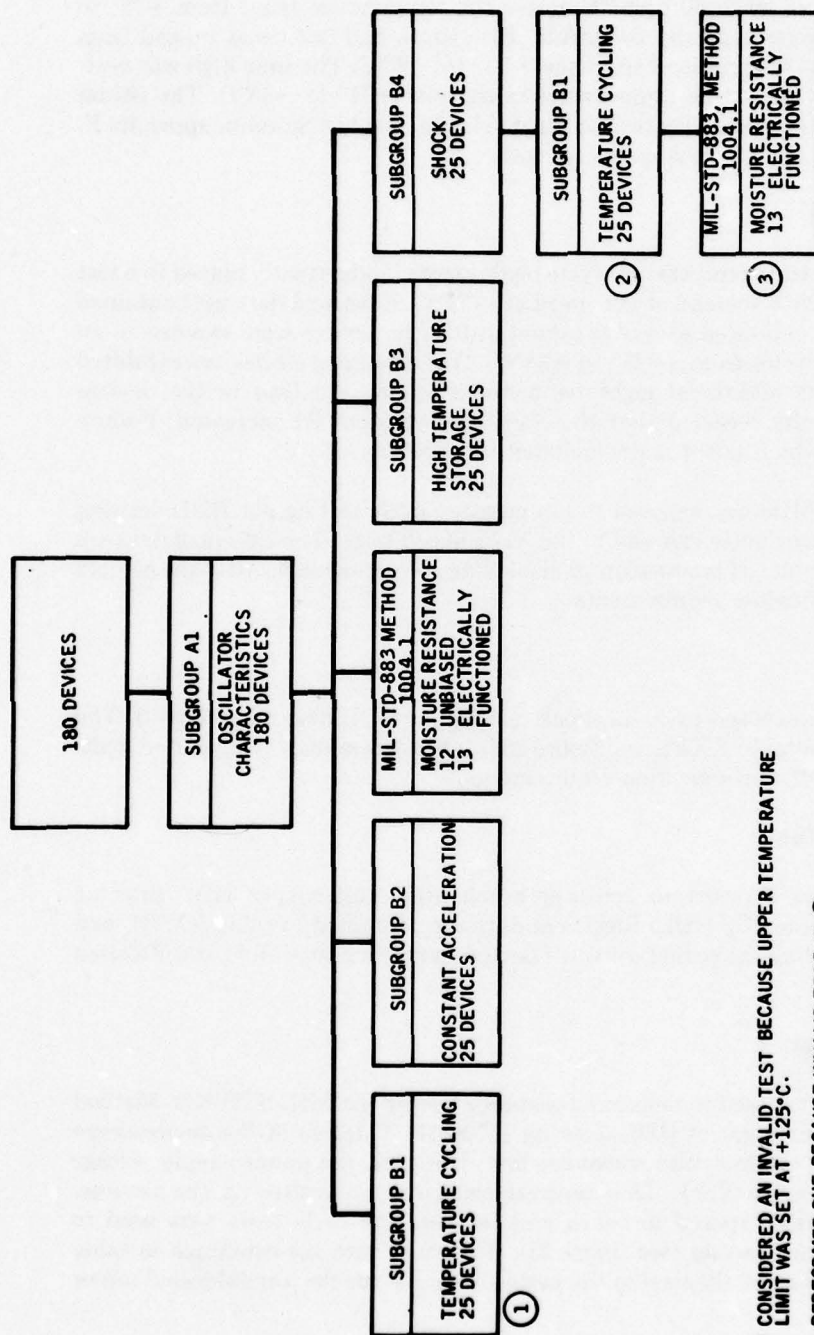


Figure 22. Histograms of period change through 57-mm testing.



- ① CONSIDERED AN INVALID TEST BECAUSE UPPER TEMPERATURE LIMIT WAS SET AT +125°C.
- ② PERFORMED DUE BECAUSE INVALID TEST IN ①.
- ③ PERFORMED BECAUSE 13 DEVICES PLACED IN MOISTURE RESISTANCE TESTING ORIGINALLY WERE BIASED INCORRECTLY AND ELECTRICALLY OVERSTRESSED.

Figure 23. Flow diagram of electrical and environmental testing of 180 TAB HMOs.

Group A electrical test results revealed that the 10-kHz TAB HMO performed well within the specification requirements. The TCT characteristics are displayed on histograms in appendix E. The oscillator TCT ranged from 30 to 40 ppm/°C across the temperature range from +71° to -55°C. The supply currents were typically 2.0 mAdc. Rise times and fall times ranged from 200×10^{-9} to 400×10^{-9} s across the temperature range + 71° to -50°C. The time high was typically 48×10^{-6} to 52×10^{-6} s across the temperature range from +71° to -55°C. The period changes noted during the voltage sensitivity testing are displayed on a histogram in appendix F. No failures were noted during the group A electrical tests.

3.6.1 Temperature Cycle Test

Twenty-five TAB HMOs exposed to temperature cycle testing were inadvertently placed in a test where the upper limit was +125°C instead of the specified +71°C. Electrical data are contained in table XXIV. Three devices exhibited excessive period drift. The devices were exposed to an additional eight temperature cycles from +125° to -55°C. The remaining 22 devices exhibited minor period drifts during the additional eight temperature cycles. Analysis of the devices exhibiting excessive period drifts revealed that the resistance value of R1 increased. Failure analysis of the three devices which failed is documented in appendix G.

Another sample of 25 TAB HMOs was exposed to temperature cycle testing per HDL drawing 11726813 (these devices were previously exposed to the 30-kg shock test). The electrical data are contained in table XXV, and figure 24 is a histogram displaying the period drift. All of the devices meet the $\pm 250 \times 10^{-9}$ s specification requirements.

3.6.2 Shock Test

Twenty-five TAB HMOs were exposed to 30-kg shock testing per HDL drawing 11726813. The electrical data are contained in table XXVI, and figure 25 is a histogram displaying period drift. All devices met the $\pm 20 \times 10^{-9}$ s specification requirements.

3.6.3 Constant Acceleration Test

Twenty-five TAB HMOs were exposed to constant acceleration testing per HDL drawing 11726813. This test was performed by HDL. Electrical data are contained in table XXVII, and figure 26 is a histogram displaying the period drift. All devices met the $\pm 50 \times 10^{-9}$ s specification requirement.

3.6.4 Moisture Resistance Test

Twenty-five TAB HMOs were exposed to moisture resistance testing per MIL-STD-883, Method 1004.1. This test is not a requirement of HDL drawing 11726813. Thirteen of the devices were electrically functioning during the moisture resistance test. However, the power supply voltage was inadvertently reversed (+23.5 Vdc). This reversal electrically overstressed the devices. Thirteen TAB HMOs previously exposed to shock and temperature cycle tests were used to complete the moisture resistance testing (see figure 23). Electrical data are contained in table XXVIII, and figure 27 is a histogram displaying the period drift. All the devices exhibited minor period drifts.

TABLE XXIV. TEMPERATURE CYCLE TEST DATA (+125° to -55°C)

SN	T Pretest (10 ⁻⁶ s)	After 8 Cycles		After 16 Cycles	
		T (10 ⁻⁶ s)	ΔT (10 ⁻⁹ s)	T (10 ⁻⁹ s)	ΔT (10 ⁻⁹ s)
1	103.0217	103.0406	+18.9	103.0020	-38.0
2	99.4246	99.4268	+2.2	99.4117	-15.1
3	99.2337	99.8654 ¹	+631.7	-	-
4	100.2282	100.2316	+3.4	100.2337	-2.1
5	101.8024	101.8090	+6.6	101.7952	-13.8
6	98.8660	98.8895	+23.5	98.8792	-10.3
7	96.9680	96.9884	+20.4	96.9693	-19.4
8	100.8871	100.9051	+18.0	100.9710	+65.9
9	96.7969	96.8178	+20.9	96.8092	-8.6
10	97.2305	97.2530	+22.5	97.2482	-4.8
11	96.7687	96.7698	+1.1	96.7605	-9.3
13	99.1357	99.1464	+10.7	99.1407	-5.7
14	97.0150	98.6575 ¹	+1.64 x 10 ⁻⁶ s	-	-
15	97.5416	97.5485	+6.9	97.5406	-7.9
18	99.4248	99.4565	+31.7	99.4439	-12.6
19	97.2168	97.2437	+26.9	97.2396	-4.1
20	97.5055	97.5315	+26.0	97.5226	-8.9
21	96.9474	96.9596	+12.2	96.9594	-0.2
22	98.5237	98.5453	+12.6	98.5349	-10.4
24	97.0847	97.1154	+30.7	97.1116	-3.8
25	98.9142	98.9391	+24.9	98.9301	-9.0
26	98.7886	98.8117	+23.1	98.8076	-4.1
27	97.3974	97.4051	+7.7	97.4036	-1.5
28	97.0726	97.0927	+20.1	97.0885	-4.5
29	98.5339	100.8904	+2.36 x 10 ⁻⁶ s	-	-

1 Exhibits excessive period drift

TABLE XXV. TEMPERATURE CYCLE TEST DATA (+71° to -55°C)

SN	T Pretest (10 ⁻⁶ s)	T Post-test (10 ⁻⁶ s)	ΔT (10 ⁻⁹ s)
113	97.2878	97.2838	-4.0
117	98.9704	98.9612	-9.2
118	100.9021	100.9038	+1.7
119	100.5530	100.5517	-1.3
120	99.4740	99.4724	-1.6
121	97.1327	97.1287	-4.0
122	100.5480	100.5412	-6.8
123	97.6068	97.6023	-4.5
124	97.0560	97.0552	-0.8
125	98.4590	98.4576	-1.4
126	100.5174	100.5182	+0.8
127	100.6390	100.6407	+1.7
128	100.4144	100.4114	-3.0
129	101.1517	101.1541	+2.4
130	100.4309	100.4332	+2.4
131	98.8778	98.8799	+2.1
132	96.9546	96.9543	-0.3
133	98.9789	98.9786	-0.3
134	98.3896	98.3890	-0.6
135	98.2517	98.2509	-0.8
136	100.5459	100.5440	-1.9
137	99.7650	99.7662	+1.2
138	98.8969	98.8939	-3.0
139	99.1353	99.1384	+3.1
140	98.7467	98.7488	+2.1
			$\bar{x} = -1.04$
			$\sigma = 3.055$

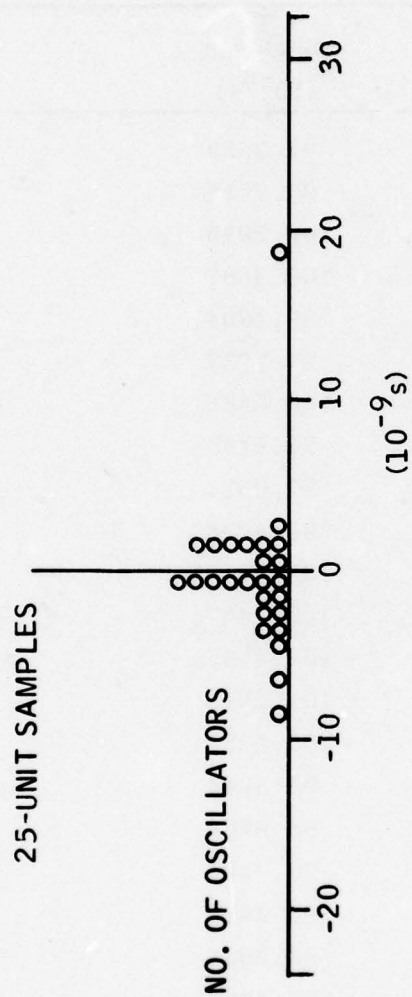


Figure 24. Histogram of period change through temperature cycle testing (+71° to -55°C).

TABLE XXVI. SHOCK TEST DATA

SN	T Pretest (10^{-6} s)	T Post-test (10^{-6} s)	ΔT (10^{-9} s)
113	97.2915	97.2925	+1.0
117	98.9733	98.9716	-1.7
118	100.9131	100.9095	-3.6
119	100.5609	100.5607	-0.2
120	99.4818	99.4804	-1.4
121	97.1361	97.1337	-2.4
122	100.5471	100.5486	+1.5
123	97.6100	97.6108	+0.8
124	97.0607	97.0614	+0.7
125	98.4626	98.4638	+1.2
126	100.5226	100.5229	+0.3
127	100.6485	100.6467	-1.8
128	100.4204	100.4186	-1.8
129	101.1593	101.1593	0
130	100.4383	100.4381	-0.2
131	98.8854	98.8844	-1.0
132	96.9613	96.9600	-1.3
133	98.9819	98.9824	+0.5
134	98.3940	98.3928	-1.2
135	98.2548	98.2586	+3.8
136	100.5463	100.5497	+3.4
137	99.7699	99.7727	+2.8
138	98.8949	98.8965	+1.6
139	99.1415	98.1431	+1.6
140	98.7527	98.7529	+0.2
			$\bar{x} = 0.112$
			$\sigma = 1.816$

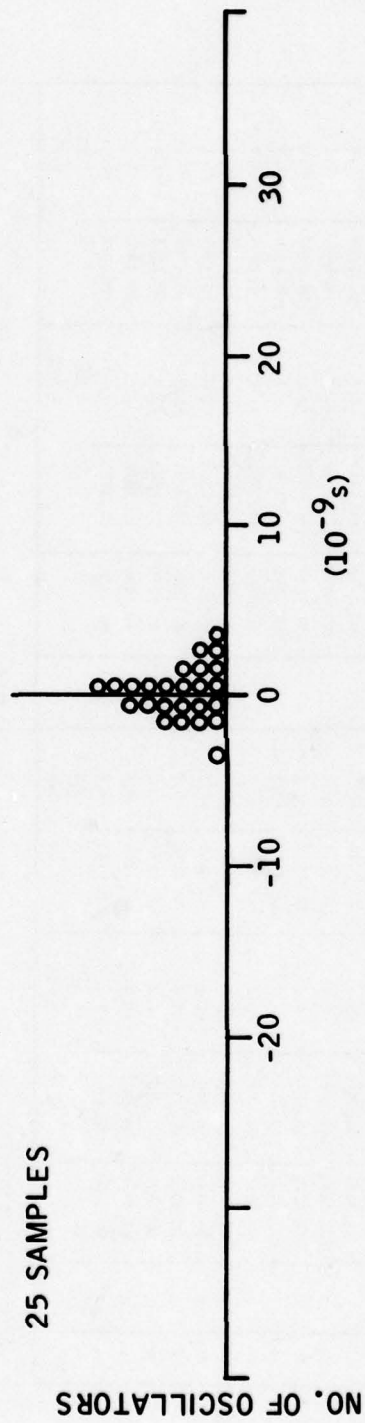


Figure 25. Histogram of period change through 30-kg shock tests.

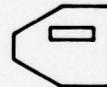
TABLE XXVII. CONSTANT ACCELERATION TEST DATA

SN	Socket ²	T Pretest (10 ⁻⁶ s)	T at 350 RPS (10 ⁻⁶ s)	ΔT B → 350 RPS (10 ⁻⁹ s)	T Post-test (10 ⁻⁶ s)	ΔT Pre to Post (10 ⁻⁹ s)	Socket (2)	T Pretest (10 ⁻⁶ s)	T at 350 RPS (10 ⁻⁶ s)	ΔT B → 350 RPS (10 ⁻⁹ s)	T Post-test (10 ⁻⁶ s)	ΔT Pre to Post (10 ⁻⁹ s)
56	2	96.5209	96.5130	-7.9	96.5209	0	3	96.5227	96.5223	-0.4	96.5240	+1.3
57	2	98.5732	98.5702	-3.0	98.5746	+1.4	3	98.5782	98.5798	+1.6	98.5794	+1.2
58	2	97.1575	97.1529	-4.6	97.1567	-0.8	3	97.1628	97.1616	-1.2	97.1639	+1.1
59	2	98.6163	98.6066	-9.7	98.6165	+0.2	3	98.6191	98.6185	-0.6	98.6203	+1.2
60	2	100.7870	100.7825	-4.5	100.7822	-4.8	3	100.7858	100.7887	+2.9	100.7866	+0.8
61	2	96.8356	96.8325	-3.1	96.8361	+0.5	3	96.8366	96.8346	-2.0	96.8377	+1.1
62	2	98.9340	98.9330	-1.0	98.9349	+0.9	3	98.9384	98.9381	-0.3	98.9388	+0.4
63	2	97.5483	97.5463	-2.0	97.5492	+0.9	3	97.5522	97.5545	+2.3	97.5536	+1.4
64	2	101.1157	101.1140	-1.7	101.1182	+2.5	3	101.1209	101.1182	-2.7	101.1217	+0.8
65	2	99.0008	98.9987	-2.1	99.0041	+3.3	3	99.0066	99.0077	+1.1	99.0078	+1.2
66	2	96.7617	96.7555	-6.2	96.7600	+1.7	3	96.7615	96.7607	-0.8	96.7621	+0.6
67	2	98.1521	98.1499	-2.2	98.1525	+0.4	3	98.1560	98.1568	+0.8	98.1557	-0.3
68	2	98.9994	98.9964	-3.0	98.9989	-0.5	3	98.9992	98.9996	+0.4	99.0003	+1.1
69	2	97.6157	97.6067	-9.0	97.6132	-2.5	3	97.6125	97.6122	-0.3	97.6149	+2.4
71	2	96.3445	96.3416	-2.9	96.3448	+0.3	3	96.3450	96.3442	-0.8	96.3454	+0.4
72	2	100.5816	100.5801	-1.5	100.5821	+0.5	3	100.5802	100.5819	+1.7	100.5820	+1.8
73	2	98.4324	98.4276	-4.8	98.4310	-1.4	3	98.4263	98.4271	+0.8	98.4283	+2.0
74	2	100.4395	100.4373	-2.2	100.4387	-0.8	3	100.4361	100.4359	-0.2	100.4378	+1.7
75	2	96.5819	96.5747	-7.2	96.5794	-2.5	3	96.5769	96.5791	+2.2	96.5789	+2.0
76	2	97.0680	97.0622	-5.8	97.0669	-1.1	3	97.0656	97.0642	-1.4	97.0667	+1.1
77	2	98.4447	98.4401	-4.6	98.4430	-1.7	3	98.4378	98.4365	-1.3	98.4392	+1.4
78	2	98.4381	98.4281	-10.0	98.4331	-5.0	3	98.4334	98.4341	+0.7	98.4338	+0.4
79	2	97.3829	97.3756	-7.3	97.3814	-1.5	3	97.3830	97.3807	-2.3	97.3834	+0.4
80	2	99.1050	99.1048	-0.2	99.1044	-0.6	3	99.1009	99.1010	+0.1	99.1022	+1.3
81	2	98.4783	98.4761	-2.2	98.4783	0.0	3	98.4752	98.4763	+1.1	98.4763	+1.1
				$\bar{x} = -4.35$ $\sigma = 2.834$					$\bar{x} = 0.056$ $\sigma = 1.471$			

¹ Test performed by HDL.

² Orientation of Hybrid Oscillator in Fixture.

Socket 2



Socket 3



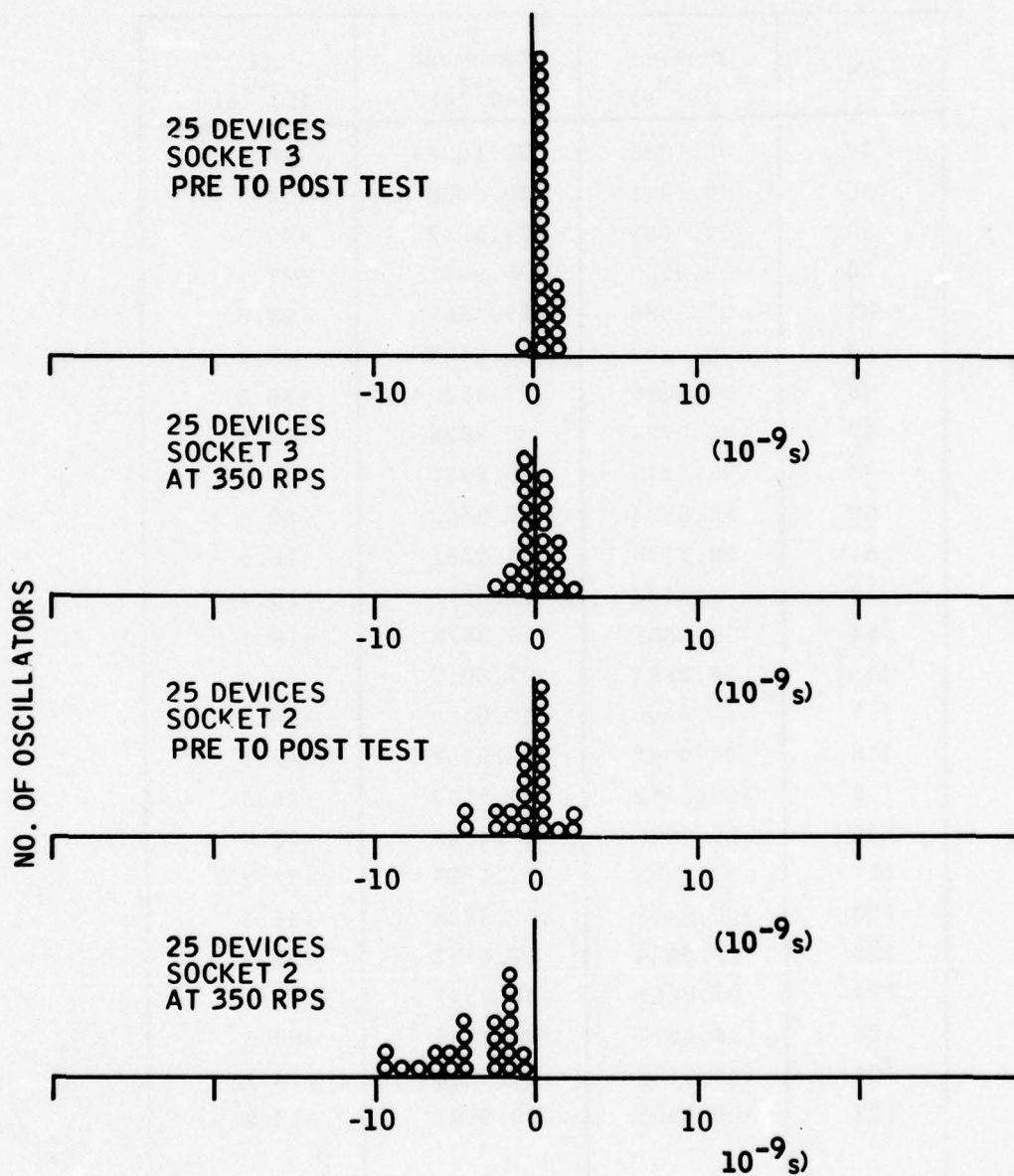


Figure 26. Histogram of period drift during constant acceleration testing.

TABLE XXVIII. MOISTURE RESISTANCE TEST DATA

SN	T Pretest (10^{-6} s)	T Post-test (10^{-6} s)	ΔT (10^{-9} s)
34	99.1028	99.1233	+20.5
36	100.6441	100.6688	+24.7
37	97.5007	97.5912	+90.5
40	99.3538	99.3811	+27.3
42	97.5086	97.5309	+22.3
44	98.5187	98.5194	+0.7
45	97.9259	97.952	+26.2
47	97.2724	97.2826	+10.3
48	98.5373	98.5641	+26.8
50	96.8174	96.8482	+30.8
51	98.2195	98.2361	+16.6
52	99.2427	99.2611	+18.4
54	98.8681	98.8872	+19.1
113 ¹	97.2884	97.3017	+13.3
117	98.9605	98.9769	+16.4
118	100.9041	100.9462	+42.1
119	100.5512	100.5780	+26.8
120	99.4725	99.4949	+22.4
121	97.1295	97.1627	+33.2
122	100.5413	100.5824	+41.1
123	97.6034	97.6357	+32.3
124	97.0561	96.9547	-101.4
125	98.4577	98.4780	+20.3
126	100.5188	100.5330	+14.2
127	100.6405	100.6587	+18.2
		$\bar{x} = +20.52$ $\sigma = 30.19$	

¹ Devices SN113 to 127 were biased with -23.5 Vdc during moisture resistance testing.

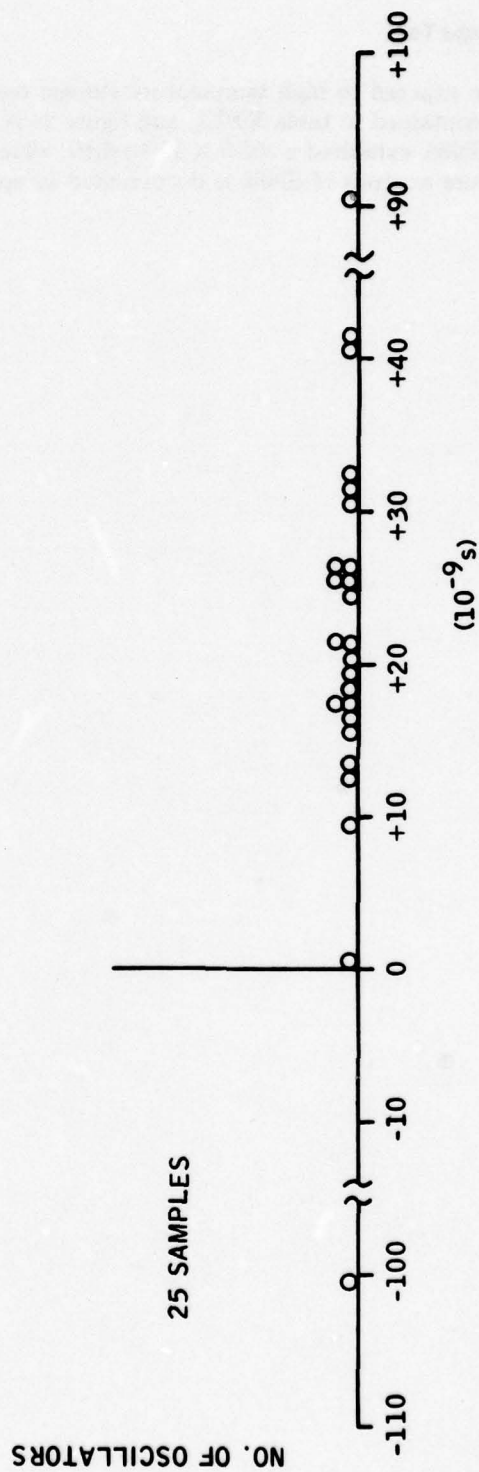


Figure 27. Histogram of period change through moisture resistance testing.

3.6.5 High Temperature Storage Test

Twenty-five TAB HMOs were exposed to high temperature storage testing per HDL drawing 11726813. Electrical data are contained in table XXIX, and figure 28 is a histogram displaying the period drift. One device, SN86, exhibited a 502.5×10^{-9} s drift, which exceeded the $\pm 250 \times 10^{-9}$ s specification limit. Failure analysis of SN86 is documented in appendix G.

TABLE XXIX. HIGH TEMPERATURE STORAGE TEST DATA

SN	T Pretest (10^{-6} s)	T Post-test (10^{-6} s)	ΔT (10^{-9} s)
82	100.9752	100.9922	17.0
83	98.6800	98.6713	-8.7
84	100.4135	100.4411	27.6
85	97.1190	97.1283	9.3
86	98.6439	99.1464	502.5 ¹
87	97.2643	97.3063	42.0
88	98.2677	98.2981	30.4
89	97.7234	97.7848	61.4
90	97.2832	97.0499	-233.3
91	102.6594	102.7122	52.8
93	98.1010	98.1426	41.6
94	98.5404	98.6138	73.4
95	99.2764	99.3313	54.9
96	98.5154	98.5637	48.3
97	101.5140	101.5737	59.7
98	99.6821	99.7403	58.2
103	99.0191	99.0442	25.1
104	100.3747	100.4210	46.3
105	98.9602	98.9883	28.1
106	97.4401	97.4931	53.0
108	99.2671	99.3023	35.2
109	97.3076	97.3072	-0.4
110	97.6938	97.7381	44.3
111	98.7137	98.7541	40.4
112	99.0514	99.1024	51.0
$\bar{x} = 27.4$ (Excludes SN86)			
$\sigma = 59.01$			

1 Period drift exceeds $\pm 250 \times 10^{-9}$ s
specification requirement.

NO. OF OSCILLATORS

25 SAMPLES
ONE DEVICE AT 502.5×10^{-9} s
ONE DEVICE AT -233.3×10^{-9} s

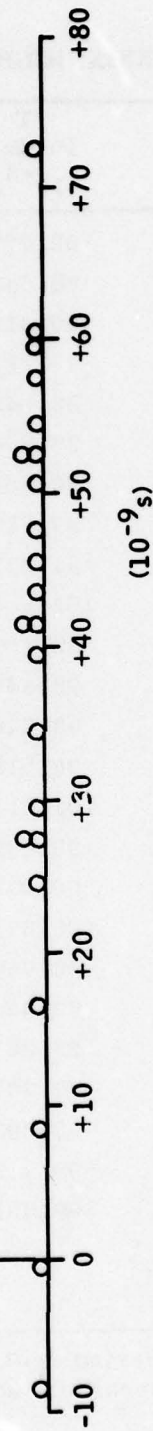


Figure 28. Histogram of period change through high temperature storage.

4. Conclusions and Recommendations

The interface monolithic integrated circuit utilizing low drop Schottky diodes to float the substrate was unacceptable for use in the XM587/724 fuze. Fabrication of this design with a dielectric isolation process should be investigated.

The Phase I and Phase II monolithic amplifier designs were incorporated in the 10-kHz TAB HMO. No significant differences were noted in the electrical characteristics of the 10-kHz TAB HMO when utilizing Phase I and Phase II monolithic amplifiers. However, a 200-kHz parasitic oscillation was noted when a failure mode was induced in the twin-T network of the 10-kHz TAB HMO. The Phase II monolithic amplifier was selected for future 10-kHz TAB HMO fabrication. The monolithic amplifiers were fabricated by one manufacturer. Another source should be developed to fabricate the monolithic amplifier.

Major elements of the 10-kHz TAB HMO are the monolithic amplifier, NPO ceramic chip capacitors, and low TCR thick film resistors which are contained on the substrate. The low TCR film resistor system is available from one manufacturer. An alternative concept or low TCR thick film resistor system should be developed as a backup for the present source.

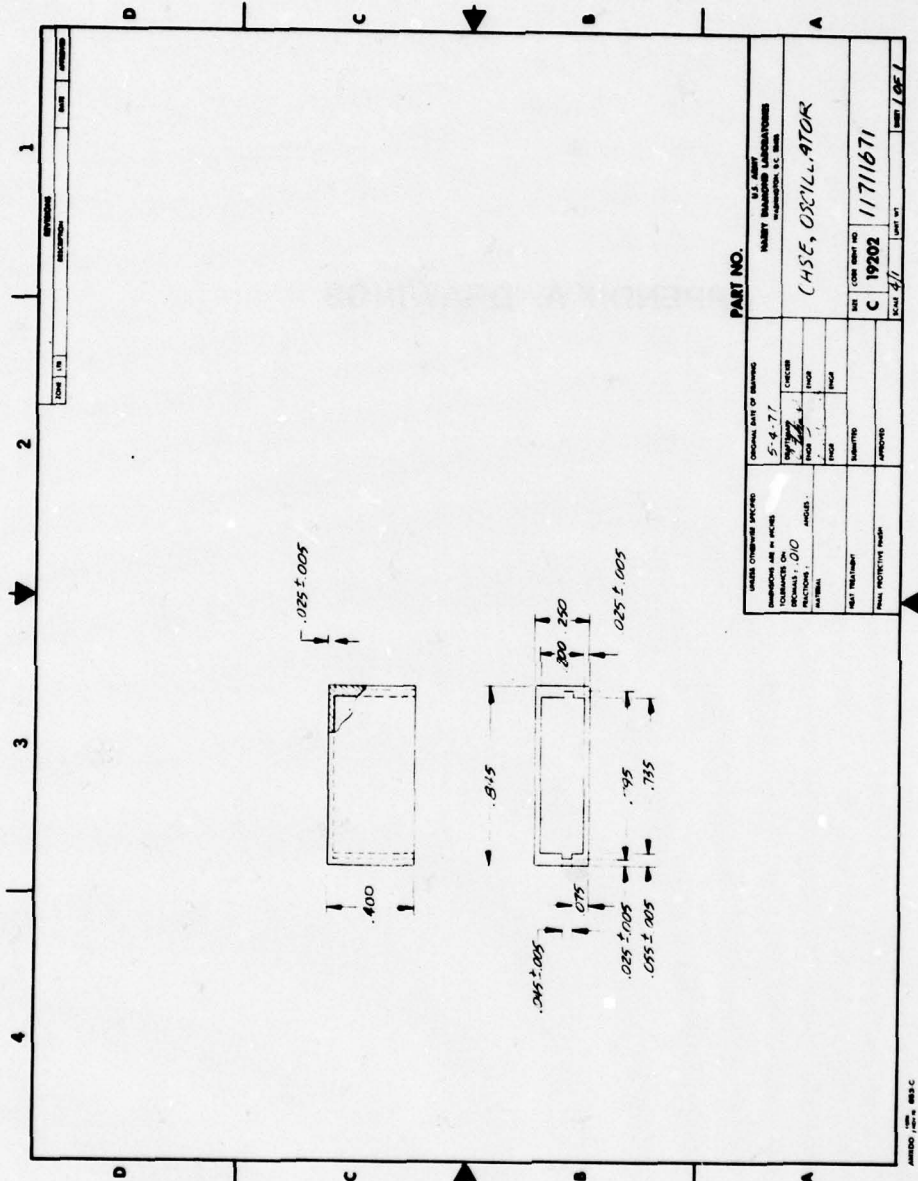
The electrical data obtained on approximately 400 TAB HMOs show that the design concept performs well within the specified requirements of HDL drawing 11726813.

Investigation of two encapsulating techniques during TAB HMO fabrication revealed superior electrical performance when a silicone barrier layer covered the substrate (i.e., solid epoxy encapsulation increased the thick film resistor TCR's by a factor of 2). Future TAB HMO fabrication will utilize a silicone barrier layer.

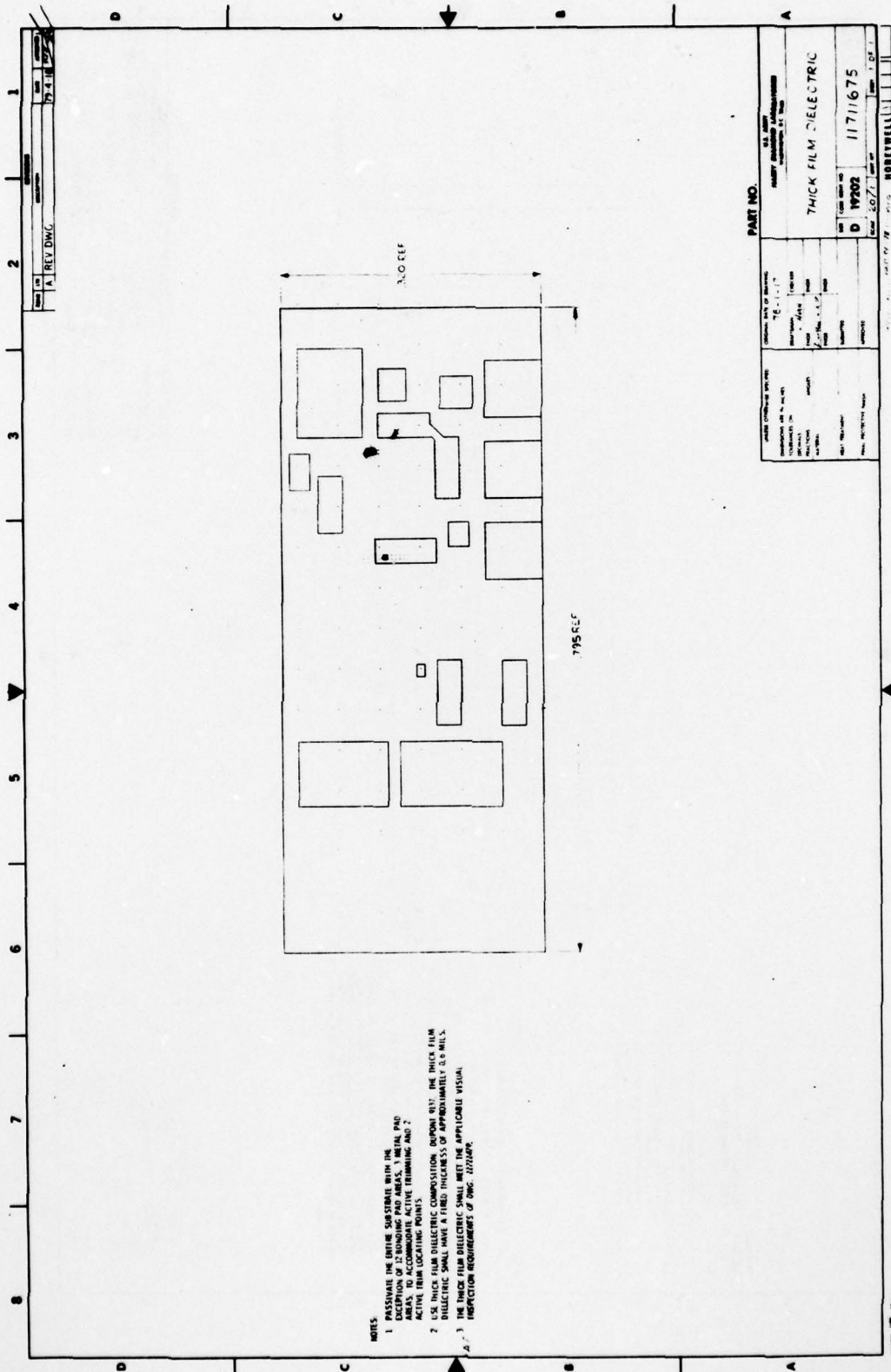
The TAB HMOs were fabricated by using a plastic case which was covered with a conductive paint to form a shield. The conductive paint exhibited cracking and crazing after exposure to an elevated temperature (+125°C) for extended periods of time (500 hr). Future TAB HMO fabrication should utilize a metal case to house the substrate and maintain reliable shielding characteristics.

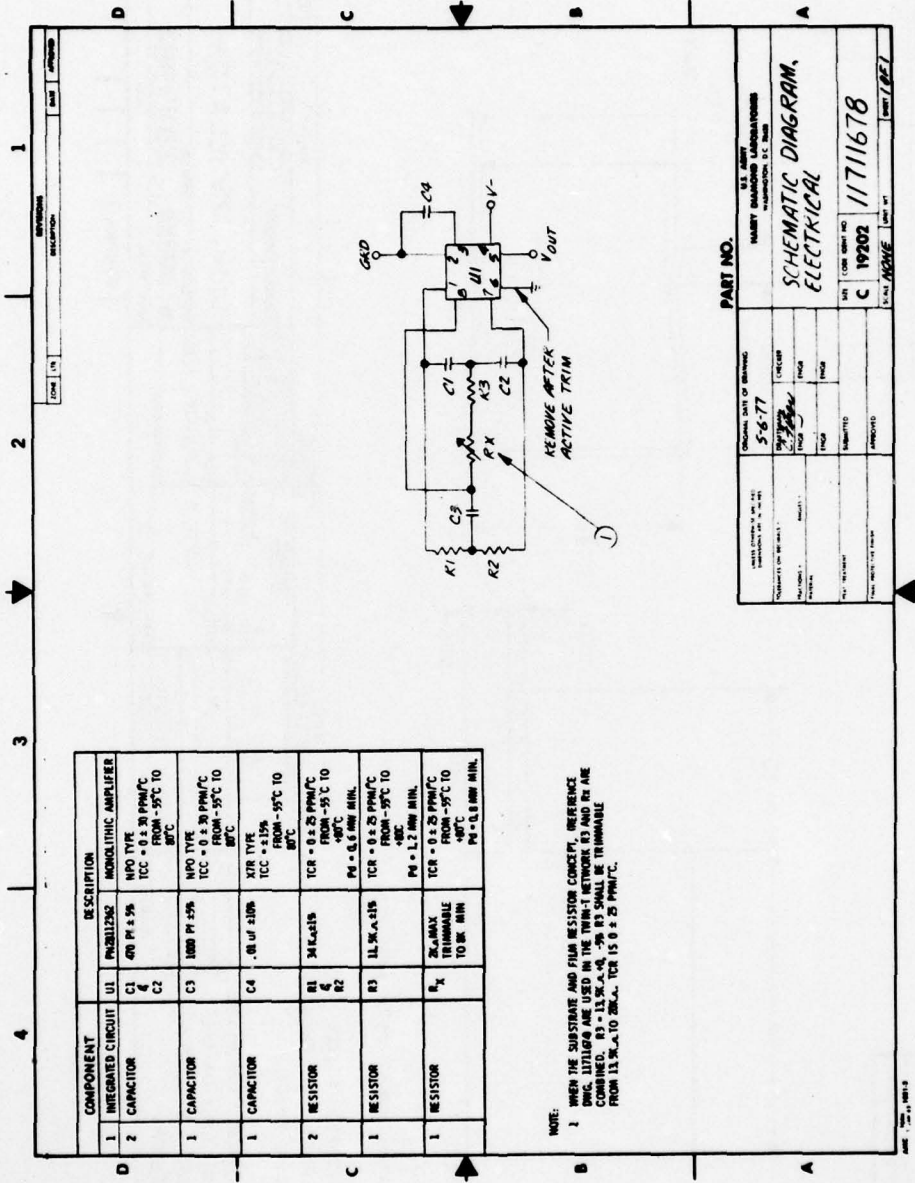
Exposure of approximately 400 TAB HMOs to temperature cycle, 30-kg shock, constant acceleration, high temperature storage, moisture resistance, and 57-mm testing revealed that the electrical and mechanical performance was well within the specified requirements of HDL drawing 11726813. The environmental testing verified that the materials selected for the 10-kHz TAB HMO design concept are electrically stable, mechanically sound, and chemically compatible.

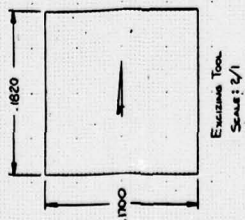
APPENDIX A. DRAWINGS









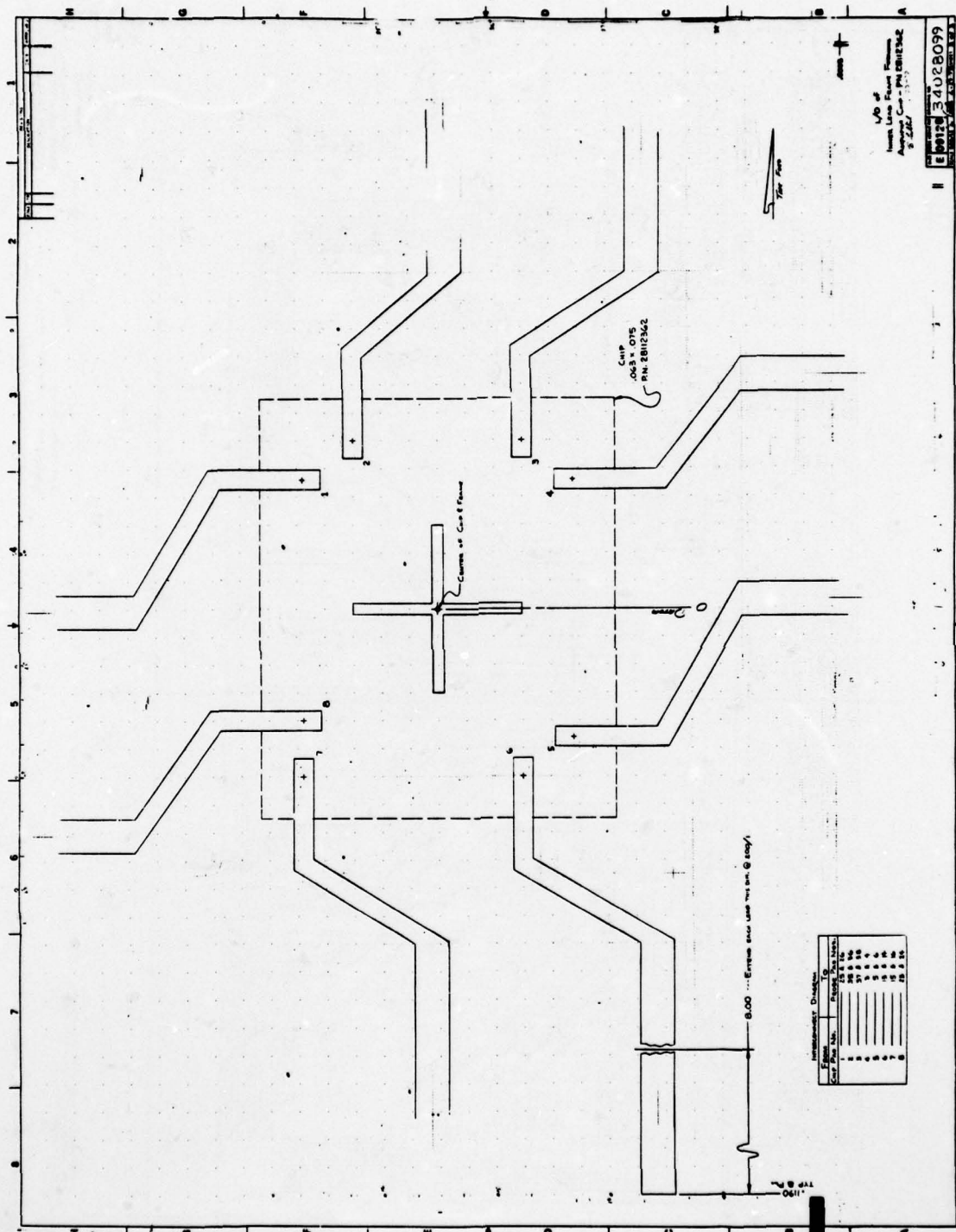


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1000 1100 FERRITE
SUPERIOR CHIP - PN 28112362

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REVISIONS																						
LTR	DESCRIPTION															DATE		APPROVED				

REV STATUS OF SHEETS	REV																					
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON: DECIMALS± FRACTIONS± ANGLES±	ORIGINAL DATE OF DRAWING		U.S. ARMY HARRY DIAMOND LABORATORIES WASHINGTON, D.C. 20438		
	DRAFTSMAN	CHECKER			
	ENGR	ENGR			
	ENGR	ENGR			
MATERIAL			INTERFACE CIRCUIT		
HEAT TREATMENT	SUBMITTED				
FINAL PROTECTIVE FINISH	APPROVED		SIZE A	CODE IDENT NO. 19202	11711670
			SCALE	UNIT WT	SHEET 1 of 24



INTERFACE CIRCUIT

1. SCOPE

1.1 Scope. This specification covers the detailed requirements for the Interface Circuit for a general purpose artillery time fuze. This circuit will be fabricated by silicon monolithic integrated circuit technology within a single package.

2. APPLICABLE DOCUMENTS

2.1 The following documents, of the issue in effect on the date of invitation for bids or request for proposal, form a part of the specification to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-M-38510 - Microcircuits, General Specification for
MIL-M-55565 - Microcircuits, Packaging of
MIL-Q-9858 - Quality Program Requirements

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics

(Copies of specifications, standards, drawings and publications required by suppliers in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer.

3. REQUIREMENTS

3.1 Samples

3.1.1 First article sample. Prior to the start of regular production, except when production on a new contract at the same facility follows within 90 days production of acceptable material under this specification, the contractor shall manufacture and submit a first article sample of 182 units using as far as possible the methods and processes proposed for quantity production. When processes differ from the production processes, they shall be basically equivalent and shall be fully described in documentation submitted with the first article sample. The sample shall conform to the requirements of this specification. Additional samples that may be required because of failure of the sample to meet the requirements of this specification shall be supplied by the contractor at his expense. Prior to approval of the first article sample, acquisition of parts and materials or initiation of production will be at the sole risk of the contractor.

3.1.2 Supplemental sample. A supplemental sample of 182 devices will be required whenever there is a change in design, material, or process which the Government Technical Agency believes may affect safety, operability, reliability or interchangeability. In all cases, such changes will require prior approval of the procuring activity.

SIZE A	CODE IDENT NO. 19202	11711670
SCALE	REV	SHEET 2

INTERFACE CIRCUIT

3.1.3 Lot acceptance sample. A test sample comprising a sufficient number of devices to meet LTPD and maximum acceptance number requirements for each test subgroup (as shown in Tables 1, 2, and 3) shall be randomly selected from each lot submitted for acceptance. Choice of the maximum acceptance number for each subgroup will require a test sample of 182 devices. Choice of less than the maximum acceptance number will permit a smaller test sample.

3.1.4 Comparison sample. Ten devices selected at random from each accepted lot (not from acceptance sample) or as specified by the Government Technical Agency shall be shipped within two working days after lot acceptance.

3.2 Construction. The device shall be constructed in accordance with the applicable drawing on sheet 20.

3.3 Performance requirements. Performance requirements cited in Tables 1, 2, and 3 of this specification are mandatory.

3.4 Markings. The following minimum markings shall apply: index point, part number, inspection lot identification code, manufacturer's identification, as described in MIL-M-38510.

3.5 Workmanship. All parts shall be manufactured and finished in a thoroughly workmanlike manner to insure satisfactory functioning and durability. (See MIL-M-38510, paragraph 3.7).

3.6 Additional requirements. The following paragraphs of MIL-M-38510 also form a part of this specification.

- 3.4.1.1 General
- 3.4.2.1 Change of product or process
- 3.5.2 Metals
- 3.5.3 Other materials
- 3.5.4 Design documentation including subparagraphs
- 3.5.5 Internal conductors
- 3.6 Marking of microcircuits including only 3.6.1,.2,.3,.4, and .8
- 3.7 Workmanship including 3.7.1 and 3.7.1.1

4. QUALITY ASSURANCE PROVISIONS

4.1 Responsibility for inspection. Unless otherwise specified in the contract or purchase order, the supplier is responsible for the performance of all inspection requirements as specified herein. Except as otherwise specified in the contract or order, the supplier may use his own or any other facilities suitable for the performance of the inspection requirements specified herein, unless disapproved by the Government. The Government reserves the right to perform any of the inspections set forth in the specification where such inspections are deemed necessary to assure supplies and services conform to prescribed requirements.

4.1.1 Contractor quality assurance system. The contractor shall provide and maintain an adequate quality assurance system in compliance with MIL-Q-9858.

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SCALE	REV	SHEET 3

INTERFACE CIRCUIT

4.2 First article sample inspection. Inspection shall be as specified in this document and referenced paragraphs of MIL-M-38510. The contractor shall notify the Government prior to proceeding with inspection to permit Government witnessing.

4.2.1 First article lot formation. The contractor shall provide 182 devices for inspection in accordance with paragraph 3.1.1.

4.2.2 First article serialization. The devices to be used for tests with electrical limits or endpoints shall be serially numbered from 1 to 158, inclusive. The remaining 24 devices to be measured for solderability, lead integrity, and external dimensions may be mechanically representative electrical rejects and are to be numbered R1 to R24, inclusive.

4.2.3 First article sample tests. The first article sample shall be examined and tested in accordance with the flow chart shown in figure 1 and the tests specified in Tables 1, 2, and 3.

4.2.4 Approval of first article sample. If the sample passes the criteria of specified examinations and tests, it shall be approved. If the sample fails in any of the examinations and tests, the failure analysis will be conducted by the contractor under Government surveillance. The results of the tests and failure analysis of the units, together with the engineering analysis of the units, shall form a basis for corrective action. Depending upon the degree of corrective action deemed necessary by the Government, the first article sample may be:

a. Accepted, provided recommended changes are made by the contractor prior to start of regular production or during production of the first lot as prescribed by the Government. In the latter case, such portions of first article sample inspections needed to verify corrective action may be included in the acceptance requirements of the lot, at the Government's discretion.

b. Rejected, and new samples for approval required for the tests failed and for related tests which might be invalidated by the corrective action.

c. Rejected, and a complete new sample required for approval.

In all cases, the contractor shall comply with any required changes to the satisfaction of the Government for the duration of the contract.

4.2.5 Reinstitution of tests. Acceptance of the first article sample does not relieve the contractor from meeting all requirements of this specification throughout the contract. The Government reserves the right to independently verify all requirements by repeating first article sample tests or any portion thereof on any production lot. If such verification indicates failure to meet requirements previously verified by first article sample tests, the contractor will be required to take corrective action. If the requirements are not met on the first lot to which the correction can be applied, the Government reserves the right to institute tightened inspection on a lot basis, by adding to the normal lot acceptance inspections all or such parts of the first article sample tests needed to verify corrective action. Normal acceptance inspection will be resumed after two consecutive lots have satisfactorily passed the tightened conditions.

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AD-A073 565

HONEYWELL INC HOPKINS MN DEFENSE SYSTEMS DIV
DEVELOPMENT OF TWO MONOLITHIC INTEGRATED CIRCUITS AND A 10-KHZ --ETC(U)
FEB 79 B GOBLISH, K CEOLA

F/G 19/1

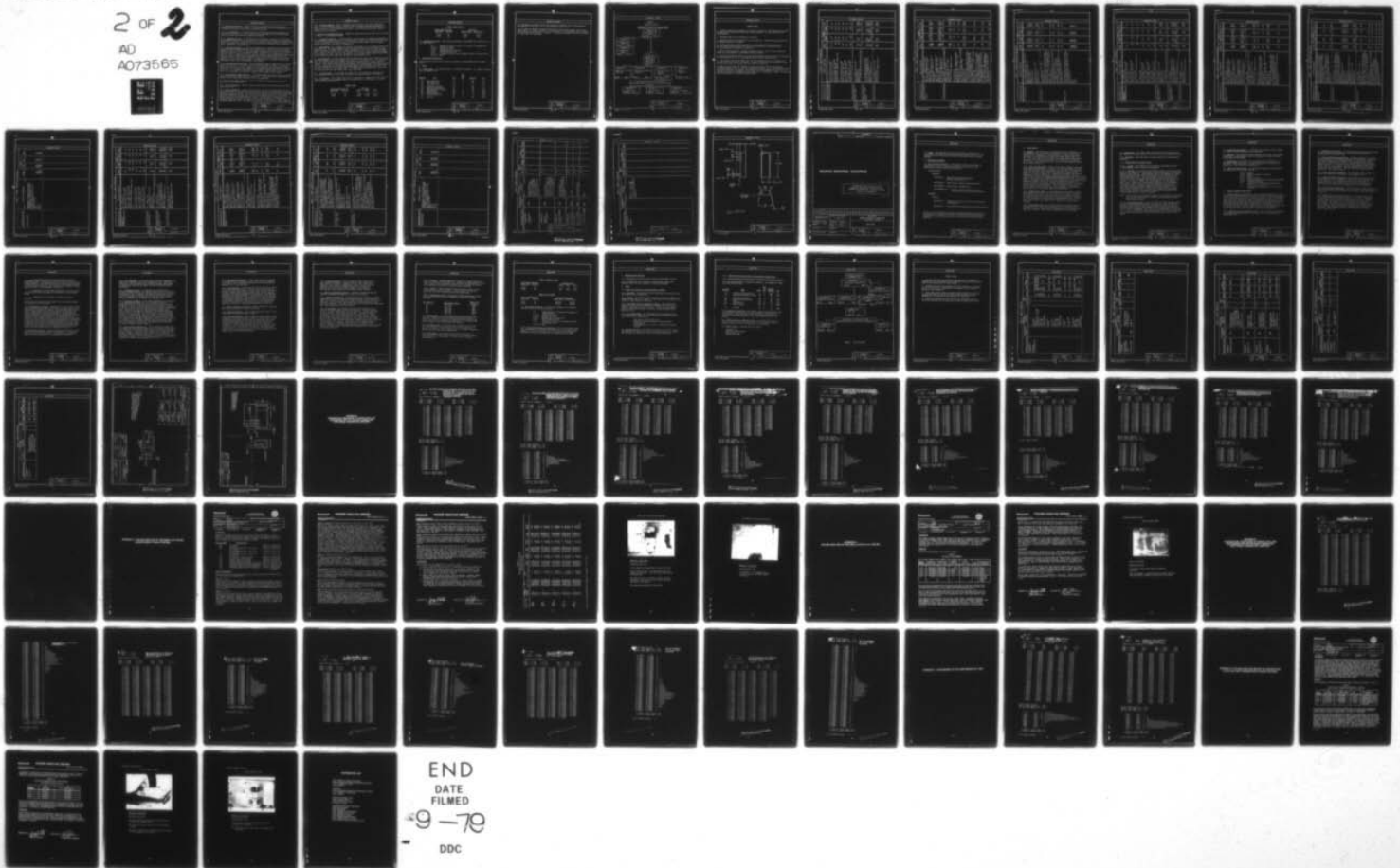
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2 OF 2
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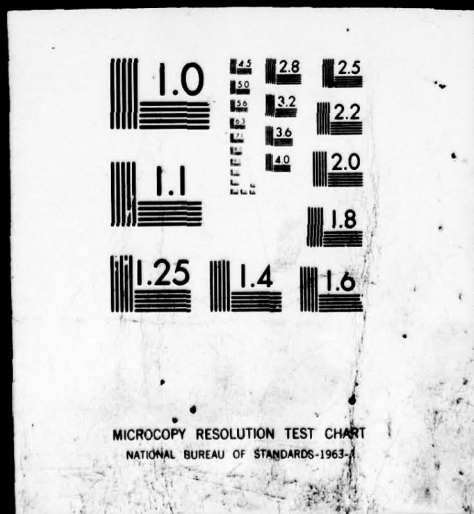
2

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2

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A073565



INTERFACE CIRCUIT

4.3 Acceptance inspection. Inspection shall be as specified in this document and referenced paragraphs of MIL-M-38510. The contractor shall notify the Government prior to proceeding with inspection to permit Government witnessing.

4.3.1 Lot information. A lot shall consist of devices produced at one manufacturing location in accordance with stabilized methods and techniques, and the same drawing and specification and revisions under continuous production.

4.3.2 Inspection lot size. An inspection lot is defined as a maximum of 20,000 devices or the quantity produced over a 30-calendar-day period whichever is smaller, presented for acceptance at one time. No minimum lot size is specified for procurements less than 50,000 units. Procurements for 50,000 units or more shall have a minimum lot size of 2000 for lot 1; 5000 for all subsequent lots.

4.3.3 Selection of sample. At the time a completed lot is presented to the Government for acceptance, the designated Government representative shall select from the lot a random sample of devices sufficient in number to conduct required tests on the lot to the maximum specified accept number for the specified LTPD. All devices to be used for tests with electrical limits or endpoints shall be serially numbered. The lot presented for acceptance shall be placed in bonded storage immediately after lot acceptance samples have been selected, and shall remain under Government control until all acceptance tests have been completed, or the lot has been rejected. All samples shall be in bonded storage except when actually under test or environmental conditioning.

4.3.4 Lot acceptance sample tests. The lot acceptance sample as specified in 3.1.3 shall be examined and tested in accordance with the flow chart shown in figure 1 and the tests specified in Tables 1, 2, and 3. Where less than 182 devices are chosen for test, the device numbers and maximum accept numbers will be adjusted accordingly with the following provisions: (1) sequence of testing will be as shown in Figure 1, and (2) all group A tests will be performed on sequentially numbered devices beginning with number 1.

4.3.5 Lot acceptance sample approval. If the sample passes the criteria of the specified examinations and tests, the lot shall be approved. If the sample fails, resubmission procedures cited in MIL-M-38510 paragraph 4.3.3.1 are applicable.

4.4 Quality conformance inspection. Quality conformance inspection shall consist of Groups A, B, and C inspections.

4.4.1 Group A inspection. Group A inspection shall consist of the examination and tests specified in Table 1.

4.4.2 Group B inspection. Group B inspection shall consist of the examination and tests specified in Table 2. Devices used for Subgroups B1, B2, and B3 inspection shall have been subjected to Subgroup A1 tests. Any device failing Subgroup A1 tests shall be removed from the Group B sample and replaced with a unit that has passed those tests. Such initial failures shall not be counted as Group B failures. Devices used for Subgroups B4, B5, and B6 may be electrically defective devices from the same production lot from which the inspection sample was drawn. They must be mechanically representative. Group B tests are considered destructive tests, and separate devices are to be used in each of the subgroups.

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INTERFACE CIRCUIT

4.4.3 Group C inspection. Group C inspection shall consist of the tests specified in Table 3. Devices used for Group C inspection shall have been subjected to Subgroup A1 tests. Any device failing Subgroup A1 tests shall be removed from the Group C sample and replaced with a unit that has passed those tests. Such initial failures shall not be counted as Group C failures.

4.5 Methods of examination and test. Methods of examination and test shall be as specified in Tables 1, 2, and 3 and as follows:

4.5.1 Inspection conditions. All measurements shall be made at TA (ambient temperature) = +25 +5°C unless otherwise specified. Test measurements shall not be started nor shall any voltages be applied to the circuit under test until the device under test has reached thermal equilibrium at the specified temperature.

4.5.2 Measurements. All voltages are measured with respect to Pin 5 (ground) unless otherwise specified. The input impedance of the instrumentation used for all output voltage measurements shall be greater than 1 megohm resistance and less than 12 picofarads capacitance. Applied test voltages shall be as specified +0.1 volt. Record actual measurements to the nearest 0.1 volt, 1 usec, or the nearest .01 milliampere unless otherwise specified. Record measurements V8A, V8AD, V8B, and V8ED to the nearest 0.01 volt.

4.6 Data recording. A written record shall be made of the results of all examinations and tests performed as specified elsewhere in section 4 of this specification. The test data shall be recorded on 80 column standard data processing punch cards, or other computer compatible input medium approved by the Government. Data from each operating test shall be recorded. Data layout of the card shall be approved by the Government. The completed cards shall be forwarded to the designated Government agency within two working days after the Government acceptance of the item or lot. If inspections are conducted on a subplot basis, the acceptance data for each subplot shall be so identified.

4.6.1 Variables data. The variables data required to be recorded for those devices in each subgroup called out in the notes to figure 1 are shown on sheets 11 through 20.

4.6.2 Data format. The variables data shall be tabulated in a format which will permit a single parameter for the complete sample to be summarized on a single page. A typical format including sample data is:

TABLE 1 TEST

Device Identification		V8A Volts		
Date Code	Unit No.	-50°C	+20°C	+71°C
75-42	21	-2.49	-2.46	-2.41
75-42	22	-2.58	-2.54	-2.50

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INTERFACE CIRCUIT

TABLES 2 AND 3 TESTS

Device Identification		V8A Volts	
Date Code	Unit No.	Before Envir.	After Envir.
75-42	51	-2.42	-2.51
75-42	52	-2.59	-2.61

4.7 Additional provisions. The following paragraphs of MIL-M-38510 also form a part of this specification.

- 4.1 Responsibility for inspection (including all subparagraphs)
- 4.3.2.1 Disposal of samples
- 4.3.2.2 Destruction tests
- 4.3.3.1 Resubmission of failed lots
- 4.3.4 Test method deviation
- 4.3.5 Procedure in case of test equipment failure or operator error
- 4.4.2.1.6 Data

5. PREPARATION FOR DELIVERY

Preparation for delivery shall conform to paragraph 5 of MIL-M-38510 and MIL-M-55565 level C.

6. NOTES

6.1 Sampling plan. The following table is included for reference. All numbers are taken from LTPD Sampling Plan.

SUBGROUP	TEST	LTPD	MAX ACC NO	QUANTITY	AQL
A1	Operational Test	5	4	158	1.3
A2	High Temperature	15	1	25	1.4
A3	Low Temperature	15	1	25	1.4
B1	Temperature Cycling	15	1	25	1.4
B2	Constant Acceleration	15	1	25	1.4
B3	High Temperature Storage	15	1	25	1.4
B4	Solderability	30	0	8	0.64
B5	Lead Integrity	30	0	8	0.64
B6	External Dimensions	30	0	8	0.64
C1	Gun Fire	10	1	38	0.94

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INTERFACE CIRCUIT

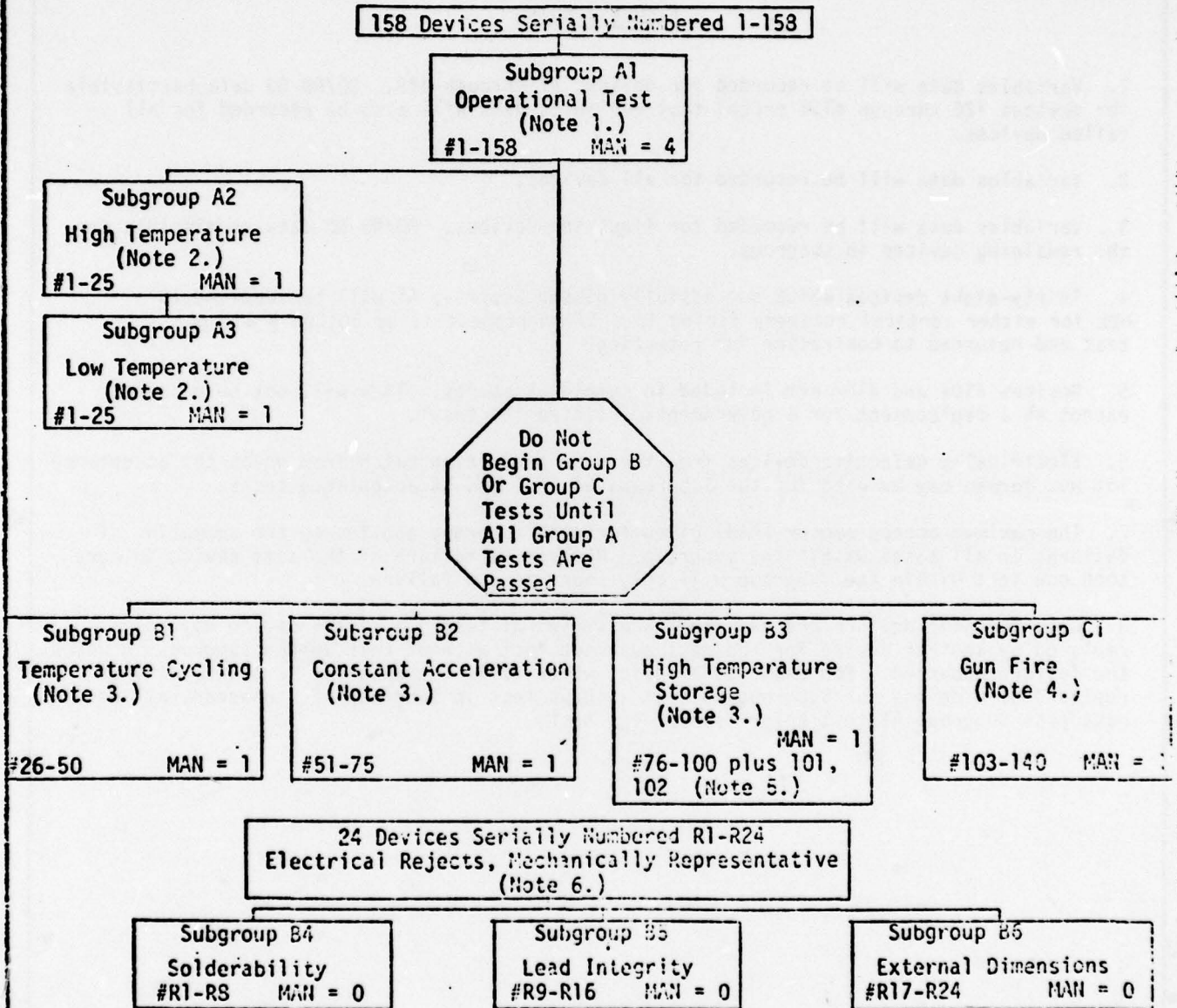
6.2 The device is designed for low cost production; therefore, only the paragraphs of MIL-M-38510 that have been cited in this document are applicable.

6.3 On sheets 11 through 19 the MIN and MAX limits refer to the absolute value of the number given. For example on sheet 17, the MIN value of -3.6 volts means that the minimum bias voltage shall be 3.6 volts or greater. This means that numbers like 3.8, 3.9, 4.0, 4.1 volts, etc. are acceptable.

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INTERFACE CIRCUIT

Figure 1
TEST FLOW CHART



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SCALE	REV	SHEET 9

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INTERFACE CIRCUIT

FIGURE 1 NOTES

1. Variables data will be recorded for devices #1 through #25. GO/NO GO data permissible for devices #26 through #158 except that variables data will also be recorded for all failed devices.
2. Variables data will be recorded for all devices.
3. Variables data will be recorded for first ten devices. GO/NO GO data permissible for the remaining devices in subgroup.
4. Thirty-eight devices which successfully passed Subgroup A1 will be supplied to HDL for either vertical recovery firing in a 57-mm projectile or 30,000 g air gun test and returned to contractor for retesting.
5. Devices #101 and #102 are included in sample as spares. They will not be measured except as a replacement for a government-certified "no test".
6. Electrically defective devices from the same production batch from which the acceptance lot was formed may be used for the Subgroups B4, B5, and B6 acceptance tests.
7. The maximum accept number (MAN) given for each subgroup applies to the summation of failures in all tests within the subgroup. However, a failure of the same device in more than one test within the subgroup will only count as one failure.
8. When the same devices are required in a series of tests, a failed device may be replaced by another device for the next subgroup test without test in the subgroup in which the failure occurred. For example, a device which fails the Subgroup A2 tests, will be replaced by a device for Subgroup A3 test without test in Subgroup A2. However, all devices must pass Subgroup A1 test before subsequent tests.

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TABLE 1: GROUP A INSPECTION

TABLE 1: GROUP A INSPECTION						
EXAMINATION OR TEST	SPECIFIC CONDITIONS	SYMBOL	LIMITS		UNIT	
			MAX	MIN		
SUBGROUP A1 (TA=25°C±2°C) Current Measurements	Pin 4 at +10V, Pin 5 at GND Measure current into Pin 4	IR 6	.90	.30	ma	
	Pin 5 at +3.0V, Pin 16 at GND Measure current into Pin 5	CSA	2.25	0.95	ma	
	Pin 5 at +30.0V, Measure current into Pin 5	CSB	3.05	1.60	ma	
	Pin 2 at +10V, Pin 3 at GND Measure current into Pin 2	IR16	2.00	1.35	ma	
	Pin 1 at +20V, Pin 3 at GND Measure current into Pin 1	IR3	1.10	0.76	ma	
	Pin 5 at GND, Pin 1 at -10V Measure current out of Pin 1	IR50	.018	.038	ma	
Positive Polarizing Voltage Circuit	Pin 5 at GND, Pin 8 at +30V Measure at Pin 9 Measure at Pin 6 Pin 7 at GND, Measure current out of Pin 7	+VP V6 IRZ	30 -0.1 .1	29.3 0.0 0.0	Volts Volts ma	
	Pin 5 at GND, Pin 16 at -27.5V Pin 8 at -27.5V Measure at Pin 9 Pin 8 at -30.0V Measure at Pin 9 Measure at Pin 15 GND Pin 8, Measure at Pin 9	V9A -VP V15 V9B	-4.2 -29.7 -27.7 V9A-0.1	-3.6 -28.9 -27.3 V9A+0.1	Volts Volts Volts Volts	
Control Line Circuit	Pin 5 at GND, Pin 3 at -4.0V Measure at Pin 7 Pin 8 at -13.0V, Measure at Pin 7	V7A V7B	-0.3 -8.6	-0.0 -7.8	Volts Volts	

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SCALE	REV	SHEET 11

INTERFACE CIRCUIT

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A

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SCALE

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SHEET 11

TABLE 1: GROUP A INSPECTION (continued)

EXAMINATION OR TEST	SPECIFIC CONDITIONS	SYMBOL	LIMITS		UNIT
			MAX	MIN	
Monitor Line Drive Circuit	301 + 1% Between Pins 8 and 5	V8A V8AD IR39	-2.00	-1.80	Volts
	3320 + 1% Between Pins 8 and 16 Pin 5 at GND, Pin 16 at -23.0V Measure at Pin 8 Pin 15 at -4.0V, Measure at Pin 8 Measure current out of Pin 15 Pin 15 open		V8A+1.65 .3	V8A+1.00 .12	
Initializing Circuit	1330 + 1% Between Pins 8 and 16	V8B V8BD IR42	-17.00	-14.90	Volts
	3320 + 1% Between Pins 8 and 5 Measure at Pin 8 Pin 6 at -3.0V, Measure at Pin 8 Measure current out of Pin 6		V8B+1.70 .25	V8B+1.05 .12	
Interface Circuit	Connect 820pf + 10% between Pins 12 and 13 Connect Pin 16 to Pin 13 Pin 5 at GND, Pin 13 at -18.0V Measure at Pin 11 Pin 13 at -21.0V, Measure at Pin 11	V11A V11B V1C	-.2 -14.0 -3.3	0.0 -9.0 -2.8	Volts Volts Volts
	Measure at Pin 9 Pin 13 and -18.0V, Voltage must change monotonically from -21.0V to -18.0V Measure at Pin 11 Pin 13 and Pin 16 open, 2000 + 1% Ω between Pins 5 and 13, Pin 14 at -24.0V Measure at Pin 11 Measure at Pin 13 Pins 14 and 13 open, Connect Pins 16 and 13, Pin 13 at -22.0V, Voltage waveform is a linear ramp between -17V and -22V with a slope of 10 V/S + 1 V/S Measure time for Pin 11 to switch between -2.0V and -7.0V	V11C V11D V13C	-.2 -18.0 -23.5	0.0 -8.0 -21.0	Volts Volts Volts
	Pin 13 open, Pin 13 at -24.0V Voltage must be applied at a rate exceeding 20V/usec, Measure delay time between -24V being applied and Pin 11 switching to a minimum of -7.0V	T11A	200.0	0.0	usec
	Pin 13 at -15.0V, voltage waveform is a step from -24V to -15V, Measure delay time between voltage step and Pin 11 crossing -2.0V	T11B	100.0	10.0	usec
		T11C	6.0	0.0	usec

TABLE 1: GROUP A INSPECTION (continued)

EXAMINATION OR TEST	SPECIFIC CONDITIONS	SYMBOL	LIMITS		UNIT
			MAX	MIN	
Fuze Power Circuit	Pin 5 at GND, 2000 \pm 1% Ω between Pins 5 and 13, Pin 14 at -50V Measure current out of Pin 14 Measure at Pin 13 Measure at Pin 1 Measure at Pin 16	I14	14.5	11.5	ma
		V13A	-25.0	-22.0	Volts
		V1A	-26.0	-22.5	Volts
		V16A	-0.1	0.0	Volts
Firing Circuit	Pin 14 open, Pin 16 at -27.0V Measure at Pin 13 Measure at Pin 3	V13B	-26.7	-26.0	Volts
		V3A	-0.1	0.0	Volts
		V4D	-0.5	0.0	Volts
		V3B	-17.0	-16.8	Volts
Schottky Diode	Pin 5 at GND, Pin 3 at -50V Measure at Pin 4 Pin 3 open, 2.00 \pm 1% noninductive ohms between Pins 5 and 4, 2.00 \pm 1% Ω between Pins 5 and 3, 56.2 \pm 1% K Ω between Pins 3 and 1, Pin 1 at -17.0V wait 200 msec Measure at Pin 3 Pin 2 at GND through 3.65 \pm 1% K Ω Measure peak pulse amplitude at Pin 4 Pin 2 open, Pin 1 at -26.0V wait 200 msec min, Pin 2 at GND through 5.11 \pm 1% K Ω , Measure peak pulse at Pin 4 Pin 6 open, wait 200 msec min, Measure at Pin 3	V4A	-17.0	-10.0	Volts
		V4B	-26.0	-12.0	Volts
		V3C	-26.0	-25.5	Volts
		ISK5 ISK8 ISK14 ISK16	550 550 550 550	100 100 100 100	MV MV MV MV

TABLE 1: GROUP A INSPECTION

EXAMINATION OR TEST	SPECIFIC CONDITIONS	SYMBOL	LIMITS		UNIT
			MAX	MIN	
SUBGROUP A2 Current Measurements	TA = 125°C + 2°C Pin 4 at +10V, Pin 5 at GND Measure current into Pin 4	IR6	.9	.3	ma
	TA = 71°C + 2°C Pin 5 at +3.0V, Pin 16 at GND Measure current into Pin 5	CSA	1.85	0.80	ma
	TA = 71°C + 2°C Pin 5 at +30.0V, Measure current into Pin 5	CSB	2.50	1.30	ma
	TA = 125°C + 2°C Pin 2 at +10V, Pin 3 at GND Measure current into Pin 2	IR16	2.0	1.30	ma
	TA = 125°C + 2°C Pin 1 at +20V, Pin 3 at GND Measure current into Pin 1	IR3	1.03	0.70	ma
	TA = 125°C + 2°C Pin 5 at GND, Pin 1 at -10V Measure current out of Pin 1	IR50	.25	.05	ma
	TA = 71°C + 2°C Pin 5 at GND, Pin 8 at +30V Measure at Pin 9 Measure at Pin 6 TA = 71°C + 2°C Pin 7 at GND, Measure current out of Pin 7	+VP V6 IRZ	30.0 -0.1 .1	29.3 0.0 0.0	Volts Volts ma
Positive Polarizing Voltage Circuit	TA = 71°C + 2°C Pin 5 at GND, Pin 16 at -27.5V Measure at Pin 9 Pin 8 at -27.5V Measure at Pin 9 Pin 8 at -30.0V Measure at Pin 9 Measure at Pin 15 GRND Pin 8, Measure at Pin 9	V9A -VP V15 V9B	-4.2 -29.7 -27.7 V 9A-0.1	-3.6 -28.9 -27.3 V 9A+0.1	Volts Volts Volts Volts
	TA = 71°C + 2°C Pin 5 at GND, Pin 8 at -4.0V Measure at Pin 7 Pin 8 at -13.0V, Measure at Pin 7	V7A V7B	-0.8 -9.3	-0.0 -8.2	Volts Volts
Negative Polarizing and Bias Voltage Circuit					
Control Line Circuit					

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ACODE IDENT NO.
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SHEET 14

TABLE 1: GROUP A INSPECTION (continued)

EXAMINATION OR TEST	SPECIFIC CONDITIONS	SYMBOL	LIMITS		UNIT
			MAX	MIN	
Monitor Line Drive Circuit	TA = 71°C + 2°C) 301 + 1% Ω Between Pins 8 and 5 3320 + 1% Ω Between Pins 8 and 16 Pin 5 at GND, Pin 16 at -23.0V Measure at Pin 8 Pin 15 at -4.0V, Measure at Pin 8 Measure current out of Pin 15 Pin 15 open 1330 + 1% Ω Between Pins 8 and 16 3320 + 1% Ω Between Pins 8 and 5 Measure at Pin 8 Pin 6 at -3.0V, Measure at Pin 8 Measure current out of Pin 6	V8A V8AD IR39	-2.00 V8A+1.70 .48	-1.80 V8A+1.05 .25	Volts Volts ma
		V8B V8BD IR42	-17.00 V8B+1.75 .38	-14.90 V8B+1.10 .20	Volts Volts ma
Initializing Circuit	TA = 125°C + 2°C) Connect 820pf + 10% between Pins 12 and 13 Connect Pin 16 to Pin 13 Pin 5 at GND, Pin 13 at -18.0V Measure at Pin 11 Pin 13 at -21.0V, Measure at Pin 11 Measure at Pin 9 Pin 13 at -18.0V, Voltage must change monotonically from -21.0V to -18.0V Measure at Pin 11 Pin 13 and Pin 16 open, 2000 \pm 1% Ω between Pins 5 and 13, Pin 14 at -24.0V Measure at Pin 11 Measure at Pin 13 Pins 14 and 13 open, Connect Pins 16 and 13, Pin 13 at -22.0V, Voltage waveform is a linear ramp between -17V and -22V with a slope of 10 V/S \pm 1V/S Measure time for Pin 11 to switch between -2.0V and -7.0V	V11A V11B	.2 -14.0	0.0 -9.0	Volts Volts
		V9C	-3.3	-2.8	Volts
		V11C	.2	0.0	Volts
		V11D V13C	-18.0 -23.5	-9.0 -21.0	Volts Volts
		T11A	200.0	0.0	usec

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ACODE IDENT NO.
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SCALE

REV

SHEET 15

TABLE 1: GROUP A INSPECTION (continued)

EXAMINATION OR TEST	SPECIFIC CONDITIONS	SYMBOL	LIMITS		UNIT
			MAX	MIN	
Initializing Circuit (continued)	Pin 13 open, Pin 13 at -24.0V. Voltage must be applied at a rate exceeding 20V/usec. Measure delay time between -24V being applied and Pin 11 switching to a minimum of -7.0V	T11B	100.0	10.0	usec
	Pin 13 at -15.0V, voltage waveform is a step from -24V to -15V. Measure delay time between voltage step and Pin 11 crossing -2.0V	T11C	6.0	0.0	usec
Fuze Power Circuit	TA = 71°C + 2°C Pin 5 at GND, 2000 + 1% Ω between Pins 4 and 13, Pin 14 at -50V. Note: (Wait 15 seconds for thermal equilibrium under the 2K load conditions before performing measurements) Measure current out of Pin 14 Measure at Pin 13 Measure at Pin 1 Measure at Pin 16 The note above does not apply for the following test Pin 14 open, Pin 16 at -27.0V Measure at Pin 13 Measure at Pin 3	14 V13A V1A V16A	14.0 -25.5 -26.0 -0.1	11.0 -22.0 -22.5 0.0	ma Volts Volts Volts
		V13B V3A	-26.7 -0.1	-26.0 0.0	Volts Volts
Firing Circuit	TA = 125°C + 2°C Pin 5 at GND, Pin 3 at -50V Measure at Pin 4 Pin 3 open, 2.00 + 1% noninductive ohms between Pins 5 and 7, 2.00 + 1% Ω between Pins 5 and 3, 56.2 + 1% K Ω between Pins 3 and 1, Pin 1 at -17.0V wait 200 msec Measure at Pin 3 Pin 2 at GND through 3.65 + 1% K Ω Measure peak pulse amplitude at pin 4 Pin 2 open, Pin 1 at -26.0V wait 200 msec min, Pin 2 at GND through 5.11 + 1% K Ω , Measure peak pulse at Pin 4 Pin 2 open, wait 200 msec min, Measure at Pin 3	V4D	-0.5	0.0	Volts
		V3B	-17.0	-16.8	Volts
		V4A	-17.0	-10.0	Volts
		V4B	-26.0	-12.0	Volts
		V3C	-26.0	-25.5	Volts

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SHEET 16

TABLE 1: GROUP A INSPECTION (continued)

EXAMINATION OR TEST	SPECIFIC CONDITIONS	SYMBOL	LIMITS		UNIT
			MAX	MIN	
Schottky Diodes	Ground each of the following pins, individually, and measure voltage at 125°C to pin 10 with a 1 ma current source into pin 10. All other pins open: Pin 5 Pin 8 Pin 14 Pin 16	ISK5	400	50	MV
		ISK8	400	50	MV
		ISK14	400	50	MV
		ISK16	400	50	MV

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A	19202	
SCALE	REV	SHEET 17



SIZE
A

CODE IDENT NO.
19202

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SCALE

REV

SHEET 17

TABLE 1: GROUP A INSPECTION

EXAMINATION OR TEST	SPECIFIC CONDITIONS	SYMBOL	LIMITS		UNIT
			MAX	MIN	
SUBGROUP A3 Current Measurements	TA = $-50^{\circ}\text{C} \pm 2^{\circ}\text{C}$ Pin 4 at +10V, Pin 5 at GND Measure current into Pin 4	IR6	.70	.30	ma
	Pin 5 at +3.0V, Pin 16 at GND Measure current into Pin 5	CSA	3.00	1.05	ma
	Pin 5 at +30.0V, Measure current into Pin 5	CSB	4.00	2.20	ma
	Pin 2 at +10V, Pin 3 at GND Measure current into Pin 2	IR16	2.15	1.45	ma
	Pin 1 at +20V, Pin 3 at GND Measure current into Pin 1	IR3	1.15	.83	ma
	Pin 5 at GND, Pin 1 at -10V Measure current out of Pin 1	IR50	.25	.05	ma
Positive Polarizing Voltage Circuit	TA = $-50^{\circ}\text{C} \pm 2^{\circ}\text{C}$ Pin 5 at GND, Pin 8 at +30V Measure at Pin 9 Measure at Pin 6 Pin 7 at GND, Measure current out of Pin 7	+VP V6 IRZ	30.0 -0.1 .1	29.3 0.0 0.0	Volts Volts ma
	TA = $-50^{\circ}\text{C} \pm 2^{\circ}\text{C}$ Pin 5 at GND, Pin 16 at -27.5V Pin 8 at -27.5V Measure at Pin 9 Pin 8 at -30.0V Measure at Pin 9 Measure at Pin 15 GRND Pin 8, Measure at Pin 9	V9A -VP V15 V9B	-4.2 -29.7 -27.7 V 9A-0.1	-3.6 -28.9 -27.3 V 9A+0.1	Volts Volts Volts Volts
	Pin 5 at GND, Pin 8 at -4.0V Measure at Pin 7 Pin 8 at -13.0V, Measure at Pin 7 TA = $-50^{\circ}\text{C} \pm 2^{\circ}\text{C}$	V7A V7B	-0.1 -7.6	0.0 -7.0	Volts Volts
Control Line Circuit					

SIZE

A

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11711670

SCALE

REV

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TABLE 1: GROUP A INSPECTION (continued)

TABLE 1: GROUP A INSPECTION (continued)					
EXAMINATION OR TEST	SPECIFIC CONDITIONS	SYMBOL	LIMITS		UNIT
			MAX	MIN	
Monitor Line Drive Circuit	TA = -50°C + 2°C 301 + 1%Ω between Pins 8 and 5 3320 + 1%Ω between Pins 8 and 16 Pin 5 at GND, Pin 16 at -23.0V Measure at Pin 8 Pin 15 at -4.0V, Measure at Pin 8 Measure current out of Pin 15 Pin 15 open 1330 + 1%Ω between Pins 8 and 16 3320 + 1%Ω between Pins 8 and 5 Measure at Pin 8 Pin at -3.0V, Measure at Pin 8 Measure current out of Pin 6	V8A V8AD IR39	-2.00 V8A+1.60 .25	-1.8 V8A+0.95 .1	Volts Volts ma
		V8B V8BD IR42	-17.00 V8B+1.65 .20	-14.90 V8B+0.95 .10	Volts Volts ma
Initializing Circuit	TA = -50°C + 2°C Connect 820pf + 10% between Pins 12 and 13 Connect Pin 13 to Pin 16 Pin 5 at GND, Pin 13 at -18.0V Measure at Pin 11 Pin 13 at -21.0V, Measure at Pin 11 Measure at Pin 9 Pin 13 at -18.0V, Voltage must change monotonically from -21.0V to -18.0V Measure at Pin 11 Pin 13 and Pin 16 open, 2000 + 1%Ω between Pins 5 and 13, Pin 14 at -24.0V Measure at Pin 11 Measure at Pin 13 Pins 14 and 13 open, Connect Pins 13 and 16, Pin 13 at -22.0V, Voltage waveform is a linear ramp between -17V and -22V with a slope of 10 V/S + 1 V/S Measure time for Pin 11 to switch between -2.0V and -7.0V	V11A V11A	.2 -14.0	0.0 -9.0	Volts Volts
		V9C	-3.3	-2.8	Volts
		V11C	.2	0.0	Volts
		V11D V13C	-18.0 -23.5	-8.0 -21.0	Volts Volts
		T11	200.0	0.0	usec

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INTERFACE CIRCUIT

TABLE 1: GROUP A INSPECTION (continued)

EXAMINATION OR TEST	SPECIFIC CONDITIONS	SYMBOL	LIMITS		UNIT
			MAX	MIN	
Initializing Circuit TA = -50°C ± 2°C	Pin 13 open, Pin 13 at -24.0V Voltage must be applied at a rate exceeding 20V/usec, Measure delay time between -24V being applied and Pin 11 switching to a minimum of -7.0V	T11B	100.0	10.0	usec
	Pin 13 at -15.0V, voltage waveform is a step from -24V to -15V, Measure delay time between voltage step and Pin 11 crossing -2.0V	T11C	6.0	0.0	usec
Fuze Power Circuit TA = -50°C ± 2°C	Pin 5 at GND, 2000 + 1% Ω between Pins 5 and 13, Pin 14 at -50V Measure current out of Pin 14 Measure at Pin 13 Measure at Pin 1 Measure at Pin 16	I14 V13A V1A V16A	15.5 -25.0 -26.0 -0.1	11.0 -22.0 -22.5 0.0	ma Volts Volts Volts
	Pin 14 open, Pin 16 at -27.0V Measure at Pin 13 Measure at Pin 3	V13B V3A	-26.7 -0.1	-26.0 0.0	Volts Volts
Firing Circuit TA = -50°C ± 2°C	Pin 5 at GND, Pin 3 at -50V Measure at Pin 4 Pin 3 open, 2.00 + 1% noninductive ohms between Pins 5 and 4, 2.00 + 1% uf between Pins 5 and 3, 56.2 + 1% KΩ between Pins 3 and 1, Pin 1 at -17.0V wait 200 msec Measure at Pin 3 Pin 2 at GND through 3.65 + 1% KΩ Measure peak pulse amplitude at Pin 4 Pin 2 open, Pin 1 at -26.0V wait 200 msec min, Pin 2 at GND through 5.11 + 1% KΩ, Measure peak pulse at Pin 4 Pin 2 open, wait 200 msec min. Measure at Pin 3	V4D V3B V4A V4B V3C	-0.5 -17.0 -17.0 -26.0 -26.0	0.0 -16.8 -10.0 -12.0 -25.5	Volts Volts Volts Volts Volts
	INTERFACE CIRCUIT				

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SIZE
ACODE IDENT NO.
19202

11711670

SCALE

REV

SHEET 20

TABLE 1: GROUP A INSPECTION (continued)

INTERFACE CIRCUIT					
EXAMINATION OR TEST	SPECIFIC CONDITIONS	SYMBOL	LIMITS		UNIT
			MAX	MIN	
Schottky Diodes	Ground each of the following pins, individually, and measure voltage at 125°C to pin 10 with a 1 ma current source into pin 10. All other pins open: Pin 5 Pin 8 Pin 14 Pin 16	ISK5	650	100	MV
		ISK8	650	100	MV
		ISK14	650	100	MV
		ISK16	650	100	MV

SIZE
A

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TABLE 2: GROUP B INSPECTION

EXAMINATION OR TEST		MIL-STD-883 METHOD	CONDITIONS SPECIFIC CONDITIONS	LTPD	MAX ACC NO	SYMBOL	LIMITS		UNIT
							MAX	MIN	
SUBGROUP B1	TEMPERATURE CYCLING	1010	TEST CONDITION A EXCEPT STEP 3 TEMP IS 75°C 12 AND STEPS 1 AND 3 STABILIZATION TIMES 15 MINUTES. SAME TESTS AND LIMITS AS SUBGROUP A1	15	1				
SUBGROUP B2	CONSTANT ACCELERATION	2001	TEST CONDITION E ORIENTATION V1, Z1 (V1 ORIENTATION FORCES THE COMPONENTS AWAY FROM THE HEADER) SAME TESTS AND LIMITS AS SUBGROUP A1	15	1				
SUBGROUP B3	HIGH TEMPERATURE STORAGE	1008	TEST CONDITION C TEST DURATION 500 HRS SAME TESTS AND LIMITS AS SUBGROUP A1	30	1				
SUBGROUP B4	SOLDERABILITY	2003	ALL PINS	30	0				
SUBGROUP B5	LEAD INTEGRITY	2004	TEST CONDITION B2	30	0				
SUBGROUP B6	EXTERNAL DIMENSIONS	2009	SHEET	30	0				

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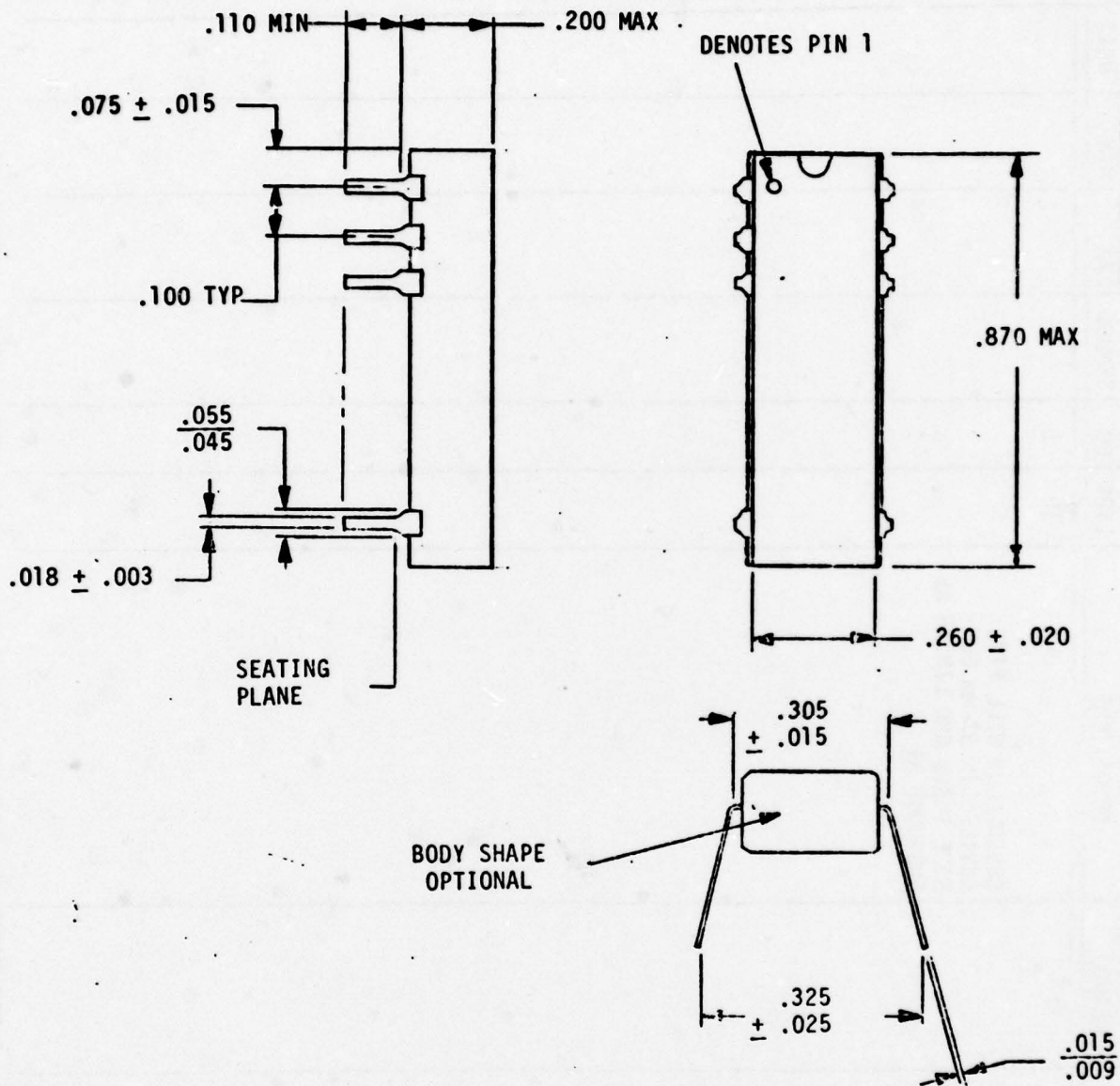
TABLE 3: GROUP C INSPECTION

EXAMINATION OR TEST	MIL-STD-883 METHOD	CONDITIONS SPECIFIC CONDITIONS	LTPD	MAX ACC NO	SYMBOL	LIMITS		UNIT
						MAX	MIN	
SUBGROUP C1 GUNFIRE		COVERED BY WILL FIRE DEVICES IN 57-INCH GUN SAME TESTS AND LIMITS AS SUBGROUP A1	10	1				

INTERFACE CIRCUIT

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SCALE	1/2	SHEET 23

INTERFACE CIRCUIT



$$R_{\theta JA} = 100^{\circ}\text{C/W (TYP)}$$

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REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

APPROVED

THIS DOCUMENT HAS BEEN RELEASED FOR
PRELIMINARY PROCUREMENT INITIATED BY HARRY
DIAMOND LABORATORIES AND IS SUBJECT TO FINAL
REVIEW AND CORRECTION.

[illegible]

OSCILLATOR

1.1 Scope. This specification covers the detail requirements for a precision oscillator for a general purpose artillery time fuze. The oscillator will be fabricated by hybrid technologies within a single package.

2. APPLICABLE DOCUMENTS

2.1 The following documents, of the issue in effect on the date of invitation for bids or request for proposal, form a part of the specification to the extent specified herein.

SPECIFICATIONS

MILITARY

- MIL-A-2550 - Ammunition and Special Weapons,
General Specification for
- MIL-M-38510 - Microcircuits, General Specification for
- MIL-M-55565 - Microcircuits, Packaging of
- MIL-Q-50829 (MU) - Quality Assurance Provisions for
Proximity Fuzes and Related Components

STANDARDS

MILITARY

- MIL-STD-105 - Sampling Procedures and Tables For Inspection
by Attributes
- MIL-STD-883 - Test Methods and Procedures for Microelectronics

(Copies of specifications, standards, drawings and publications required by suppliers in connection with specific procurement function should be obtained from the procuring activity or as directed by the contracting officer.)

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3. REQUIREMENTS

3.1 Samples. The contractor is responsible for all requirements for providing and testing of samples as prescribed herein. When this specification is assigned to a subcontractor, it shall be the prime contractor's responsibility to insure that sample requirements are met. The prime contractor shall notify the Government at the time of assignment to a subcontractor whether the testing will be performed by the prime or by the subcontractor, as well as the method of control by the prime contractor.

3.1.1 First article sample. Prior to the start of regular production, except when production on a new contract at the same facility follows within 90 days production of acceptable material under this specification, the contractor shall manufacture and submit a first article sample of 174 units using as far as possible the methods and processes proposed for quantity production. When processes differ from the production processes, they shall be basically equivalent and the difference shall be fully described in documentation submitted with the first article sample. The sample shall conform to the requirements of this specification. Additional samples that may be required because of failure of the sample to meet the requirements of this specification shall be supplied by the contractor at his expense. Prior to approval of the first article sample, acquisition of parts and materials or initiation of production will be at the sole risk of the contractor.

3.1.2 Supplemental sample. At the Government's discretion a supplemental sample of 174 units may be required whenever there is a break in production continuity of 90 days or more, or a change in design, material or process which may affect safety, operability, reliability, or interchangeability as defined by the Requirements (3.3). In all cases, such changes will require prior approval of the procuring activity.

3.1.3 Comparison sample. Ten devices selected at random from each accepted lot (not from acceptance sample) or as specified by the Government Technical Agency shall be shipped within two working days after lot acceptance to the agency designated by the Government.

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3.2 Construction. The device shall be constructed in accordance with the applicable drawings (sheets 22 and 23) to the extent prescribed herein.

3.2.1 Materials. Materials shall be those specified by the applicable drawings.

3.2.2 Dimensions and technical notes.

3.2.2.1 Listed. Those dimensions and technical requirements listed in the Classification of Defects are mandatory.

3.2.2.2 Unlisted. The contractor may propose changes to characteristics shown on the drawings for the purpose of adapting the item to established manufacturing practices. Such proposals must be accompanied by evidence that the change does not affect the function of the item and that all requirements will be met. If the Government confirms the contention of the contractor, the change will be approved for the duration of the contract. In case of dispute, the characteristics of the drawings shall apply. Approval of a change under provisions of this paragraph does not relieve the contractor from establishing and maintaining an adequate quality assurance program as elsewhere required. Provisions of this paragraph shall not be used to obtain approval for use of discrepant material (i.e., produced before approval is obtained); or for design changes, which should be requested in accordance with change provisions of the contract document.

Note: It is expected that the above changes will normally be accomplished prior to the construction of the First Article Approval Sample and reflected therein.

3.2.2.3 Interchangeability. While the dimensions and tolerances shown in the drawings and specifications will generally insure satisfactory products, the contractor is notified that some selection or matching may be required to obtain combinations which provide proper function or economic use of components. The contractor is responsible for selecting combinations of tolerances within the specified limits which satisfy his process needs and also meet the specified performance and fit requirements.

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3.3 Performance requirements. Performance requirements cited in Tables 1, 2, and 3 of this specification are mandatory.

3.4 Markings. The following minimum markings shall apply: part number, inspection lot identification code and manufacturer's identifications as described in MIL-M-38510.

3.5 Workmanship. All parts shall be manufactured and finished in a thoroughly workmanlike manner to insure satisfactory functioning and durability. (See MIL-M-38510, paragraph 3.7)

3.6 Additional requirements. The following paragraphs of MIL-M-38510 also form a part of this specification.

- 3.4.1.1 General
- 3.4.2.1 Change of product or process
- 3.5.2 Metals
- 3.5.3 Other materials
- 3.5.4 Design documentation including subparagraphs
- 3.5.5 Internal conductors
- 3.6 Marking of microcircuits including only
3.6.1, .2, .3, .4 and .8
- 3.7 Workmanship including 3.7.1, 3.7.1.1 and
3.7.1.2

4. QUALITY ASSURANCE PROVISIONS

4.1 Responsibility for inspection. Unless otherwise specified in the contract or purchase order, the supplier is responsible for the performance of all inspection requirements as specified herein. Except as otherwise specified in the contract or order, the supplier may use his own or any other facilities suitable for the performance of the inspection requirements specified herein, unless disapproved by the Government. The Government reserves the right to perform any of the inspections set forth in the specification where such inspections are deemed necessary to assure supplies and services conform to prescribed requirements.

4.1.1 Contractor quality assurance system. The contractor shall provide and maintain an adequate quality assurance system in compliance with MIL-Q-50829 (MU).

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4.2 Government verification. All quality assurance operations performed by the contractor will be subject to Government verification in compliance with MIL-Q-50829 (MU).

4.3 First article sample inspection. Inspection shall be as specified in this document and referenced paragraphs of MIL-M-38510. The tests shall be performed by the contractor under the observation of the Government QA representative and/or a representative of the cognizant technical agency. The contractor shall supply complete data in reproducible form on the contractor tests and examinations of the first article approval sample units. The data and tested samples shall be delivered to the technical agency.

4.3.1 First article lot formation. The contractor shall provide 174 devices for inspection in accordance with paragraph 3.1.1.

4.3.2 First article serialization. The devices to be used for tests with electrical limits or endpoints shall be serially numbered from 1 to 158 inclusive. The remaining 16 devices to be measured for solderability and lead strength may be mechanically representative electrical rejects and are to be numbered R1 to R16, inclusive.

4.3.3 First article sample tests. The first article sample shall be examined and tested in accordance with the Performance Requirements (3.3), Material and Component Certification (4.8.1) and the flow chart shown in Figure 1.

4.3.4 Approval of first article sample. If the sample passes the criteria of specified examinations and tests, it shall be approved. If the sample fails in any of the examinations and tests, failure analysis shall be conducted by the contractor under Government surveillance. The results of the tests and failure analysis of the units, together with the engineering analysis of the units, shall form a basis for corrective action. Depending upon the degree of corrective action deemed necessary by the Government, the first article sample may be:

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a. Conditionally approved with the provisions that the recommended changes are made by the contractor prior to start of regular production or during production of the first lot as prescribed by the Government. Such portions of first article inspections needed to verify corrective action may be included in the acceptance requirements of the lot, at the Government's discretion.

b. Disapproved, and new samples required for the tests failed and for related tests which might be invalidated by the corrective action.

c. Disapproved, and a complete new sample required for approval.

In all cases, the contractor shall comply with any required changes for the duration of the contract.

4.3.5. Reinstitution of tests. Acceptance of the first article sample does not relieve the contractor from meeting all requirements of this specification throughout the contract. The Government reserves the right to independently verify all requirements by repeating first article sample tests or any portion thereof on any production lot. If such verification indicates failure to meet requirements previously verified by first article sample tests, the contractor will be required to take corrective action. If the requirements are not met on the first lot to which the correction can be applied, the Government reserves the right to institute tightened inspection on a lot basis, by adding to the normal lot acceptance inspections all or such parts of the first article sample tests needed to verify corrective action. Normal acceptance inspection will be resumed after two consecutive lots have satisfactorily passed the tightened conditions.

4.4 Acceptance inspection. Inspection shall be as specified in this document and referenced paragraphs of MIL-M-38510. The contractor shall notify the Government prior to proceeding with inspection to permit Government witnessing at the Government's discretion.

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4.4.1 Lot formulation. A lot shall consist of devices produced at one manufacturing location under the following conditions: continuous production, stabilized methods and techniques, and the same revision of drawings and specification except for those introduced without obsolescence.

4.4.2 Inspection lot size. An inspection lot is defined as a maximum of 20,000 devices or the quantity produced over a 30-calendar-day period whichever is smaller, presented for acceptance at one time. No minimum lot size is specified for procurements less than 50,000 units. Procurements for 50,000 units or more shall have a minimum lot size of 2000 for lot 1; 5000 for all subsequent lots.

4.4.3 Selection of sample. At the time a completed lot is presented to the Government for acceptance, the designated Government representative shall select from the lot a random sample of devices sufficient in number to conduct required tests (as shown in Tables 1, 2, and 3) on the lot to the maximum acceptance number for the specified LTPD. Choice of less than the maximum acceptance numbers will permit a smaller test sample as tabulated in MIL-M-38510 Table B-1. All devices to be used for tests with electrical limits or endpoints shall be serially numbered. The lot presented for acceptance shall be placed in bonded storage immediately after lot acceptance samples have been selected, and shall remain under Government control until all acceptance tests have been completed, or the lot has been rejected. All samples shall be in bonded storage except when actually under test or environmental conditioning. For sampling other than LTPD, MIL-STD-105 inspection level II applies.

4.4.4 Lot acceptance sample tests. The lot acceptance sample shall be examined and tested in accordance with the Performance Requirements (3.3), Material and Component Certification (4.8.1) and the flow chart shown in Figure 1. Where less than 174 devices are chosen for test, the device numbers and maximum accept numbers will be adjusted accordingly with the following provisions: (1) sequence of testing will be as shown in Figure 1 and (2) all group A tests will be performed on sequentially numbered devices beginning with number 1.

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4.4.5 Lot acceptance approval. If the sample passes the criteria of the specified examinations and tests, the lot shall be approved. If the sample fails, resubmission procedures cited in MIL-M-38510 paragraph 4.3.3.1 are applicable.

4.4.6 Data recording. A written record shall be made of the results of all examinations and tests performed as specified elsewhere in section 4 of this specification. The test data shall be recorded on 80 column standard data processing punch cards, or other computer compatible input medium approved by the Government. Data from each operating test shall be recorded. Data layout of the card shall be approved by the Government. The completed cards shall be forwarded to the designated Government agency within two working days after the Government acceptance of the item or lot. If inspections are conducted on a subplot basis, the acceptance data for each subplot shall be so identified. (Engineering information, section 6).

4.5 Quality conformance inspection. Quality conformance inspection shall consist of Group A, B, and C inspections.

4.5.1 Group A inspection. Group A inspection shall consist of the examinations and tests specified in table 1.

4.5.2 Group B inspection. Group B inspection shall consist of the examinations and tests specified in table 2. Devices used for Group B inspection shall have been subjected to Subgroup A1 tests. Any device failing Subgroup A1 tests shall be removed from the Group B sample and replaced with a unit that has passed Subgroup A1 requirements. Such initial failures shall not be counted as Group B failures. With the Government's permission, the solderability and lead integrity tests may be conducted with electrical rejects. Group B tests are considered destructive tests, and separate devices shall be used in each of the subgroups.

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4.5.3 Group C inspection. Group C inspection shall consist of the tests specified in table 3. Devices used for Group C inspection shall have been subjected to Subgroup A1 tests. Any device failing Subgroup A1 tests shall be removed from the Group C sample and replaced with a unit that has passed Subgroup A1 requirements. Such initial failures shall not be counted as Group C failures.

4.6 Methods of examination and test. Methods of examination and test shall be as specified in tables 1, 2, and 3 and as follows.

4.6.1 Inspection conditions. All measurements will be made at an ambient temperature of $+25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ unless otherwise specified. Test measurements shall not be started nor shall any voltages be applied to the circuit under test until the device under test has reached thermal equilibrium at the specified temperature. The manufacturer shall be responsible for establishing that thermal equilibrium has been achieved.

4.6.2 Measurements. All voltages are measured with respect to pin 2 (ground). All measurements will be made with pin 1 (shield) connected to pin 2 (ground). Measurements will be made with a supply voltage (B-) of -23.5V at pin 4 unless otherwise specified. Current is measured through pin 4 with a meter that responds to average current. Applied test voltages shall be as specified ± 0.1 volt unless otherwise specified. Record actual measurements to nearest 0.1 volt, 0.01 ma, 0.1 ohm, 0.001 inch, 0.1 μsec unless otherwise specified. Measure period within 10 seconds of application of B- voltage. Record period (1,000 period average) to nearest 0.001 μsec . External connections to pin 3 (output) shall have an impedance of not less than 10 Meg ohm in parallel with 12 pf. Terms such as maximum, minimum, increasing and decreasing refer to magnitudes of electrical quantities.

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4.6.2.1 Group A. All measurements will be made at a supply voltage of -23.5 volts unless otherwise specified. Measure rise time between -7.0V and -2.0V. Measure fall time between -2.0V and -7.0V. Measure time high at -5.0V thresholds starting at the positive going transition.

4.6.2.2 Group B. Measure periods TS1 and TS3 within one hour before acceleration and shock respectively. Measure periods TS2 and TS4 within one hour after acceleration and shock respectively.

4.6.2.3 Temperature control. Each group of period measurements listed below shall be made at the same temperature, within the tolerance specified.

<u>Test Subgroup</u>	<u>Measurement Symbols</u>	<u>Temperature Tolerance</u>
A1	TA, TJ, TG	+1°C
B1	TT1, TT2	+2°C
B2	TS1, TS2	+2°C
B3	TT3, TT4	+2°C
B4	TS3, TS4	+1°C
C1	TGA, TGB	+2°C

4.7 Data recording. A written record shall be made of the results of all examinations and tests performed as specified elsewhere in section 4. Summary scores shall be recorded for each subgroup, and these scores plus the variables data identified in 4.7.1 and in the notes to figure 1 shall be delivered with each lot.

4.7.1 Variables data. The variables data required to be recorded for those devices in each subgroup called out in the notes to figure 1 are shown in Table 1 Subgroups A1, A2; in Table 2 Subgroups B1, B2, B3, B4; and in Table 3 Subgroup C1.

4.7.2 Data format. The variables data shall be tabulated in a format which will permit a single parameter for the complete sample to be summarized on a single page. A typical format including sample data is:

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TABLE 1 SUBGROUP 1 TEST

Device Identification		Current IA, mA		
Date Code	Unit No.	-50°C	25°C	71°C
75-42	21	-2.3	-2.3	-2.6
75-42	22	-2.1	-2.2	-2.5

TABLE 2 and 3 TESTS

Device Identification		Period, Microseconds	
Date Code	Unit No.	Before Envir.	After Envir.
75-42	51	101.076	101.003
75-42	52	98.317	98.301

4.8 Additional provisions. The following paragraphs of MIL-M-38510 also form a part of this specification.

- 4.1 Responsibility for inspection (including all subparagraphs)
- 4.3.2.1 Disposal of samples
- 4.3.2.2 Destructive tests
- 4.3.3.1 Resubmission of failure lots
- 4.3.4 Test method deviation
- 4.3.5 Procedure in case of test equipment failure or operator error
- 4.4.2.1.6 Data

4.8.1 Material and component certification. Prior to acceptance under this procurement, the contractor shall demonstrate by means of certifications or statement of findings that only materials and components conforming to the item specification and drawings have been used.

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5. PREPARATION FOR DELIVERY

5.1 Preparation for delivery shall conform to MIL-M-55565, level C.

5.1.1 In addition to the contract or purchase order number, the shipping label shall make reference to this specification.

6. NOTES

6.1 Items to be included in the procurement documents.

6.1.1 Documents. Procurement documents should specify the title, date, and number of this specification.

6.1.2 Samples. The number of units should be increased to include the samples as required in 3.1.1 and 4.4.3 since they are not included in the number of units required for delivery.

6.1.3 Government testing of comparison samples. These samples are subject to retesting by the Government to insure that first article approval requirements continue to be met. Failure of these samples will not affect the acceptance of the lot, but may indicate future mandatory action.

6.1.4 Data requirements. The following data are required by this specification to be furnished to the Government and should be entered on DD Form 1423 for each contract:

First Article Test Results (4.3)
Examination and Test Records on Data Processing
Cards (4.4.6)
MIL-Q-50829 (MU), Par. 3.6.1 -- Contractor-furnished
Designs

6.2 Advisory documents. The following documents are not part of this specification, but may provide useful data to the contractor. Copies are available for reference at the Harry Diamond Laboratories.

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6.2.1 Manufacturing process report or description of manufacture.

6.2.2 Quality assurance system documents obtained from previous contracts.

6.3 The following table is included for reference. All numbers are taken from LTPD Sampling Plans.

SUBGROUP	TEST	LTPD	MAX ACC NO	MAXIMUM QUANTITY	AQL
A1	Oscillator Characteristics	5	4	158	1.3
A2	Electrostatic Shield & Visual	20	1	18	2.0
B1	Temperature Cycling	15	1	25	1.4
B3	High Temperature Storage	15	1	25	1.4
B4	Shock	15	1	25	1.4
B5	Solderability	30	0	8	0.64
B6	Lead Integrity	30	0	8	0.64
C1	Gun Fire	10	1	38	0.94

6.4 Engineering information. Upon request, copies of the data collected in the acceptance of a lot will be made available to the Government representative. Additional data or data requiring special tests, when needed for engineering purposes, will be specifically defined by the contract.

6.5 Results of Table 3, Subgroup C1 test. If the Government does not return the devices to the contractor within 30 working days, Table 3 Subgroup C1 test will not be a requirement for acceptance.

6.6 Approved Source. Approved source of supply:

Honeywell, Inc.
Defense Systems Division
600 Second St. NE
Hopkins, MN 55343

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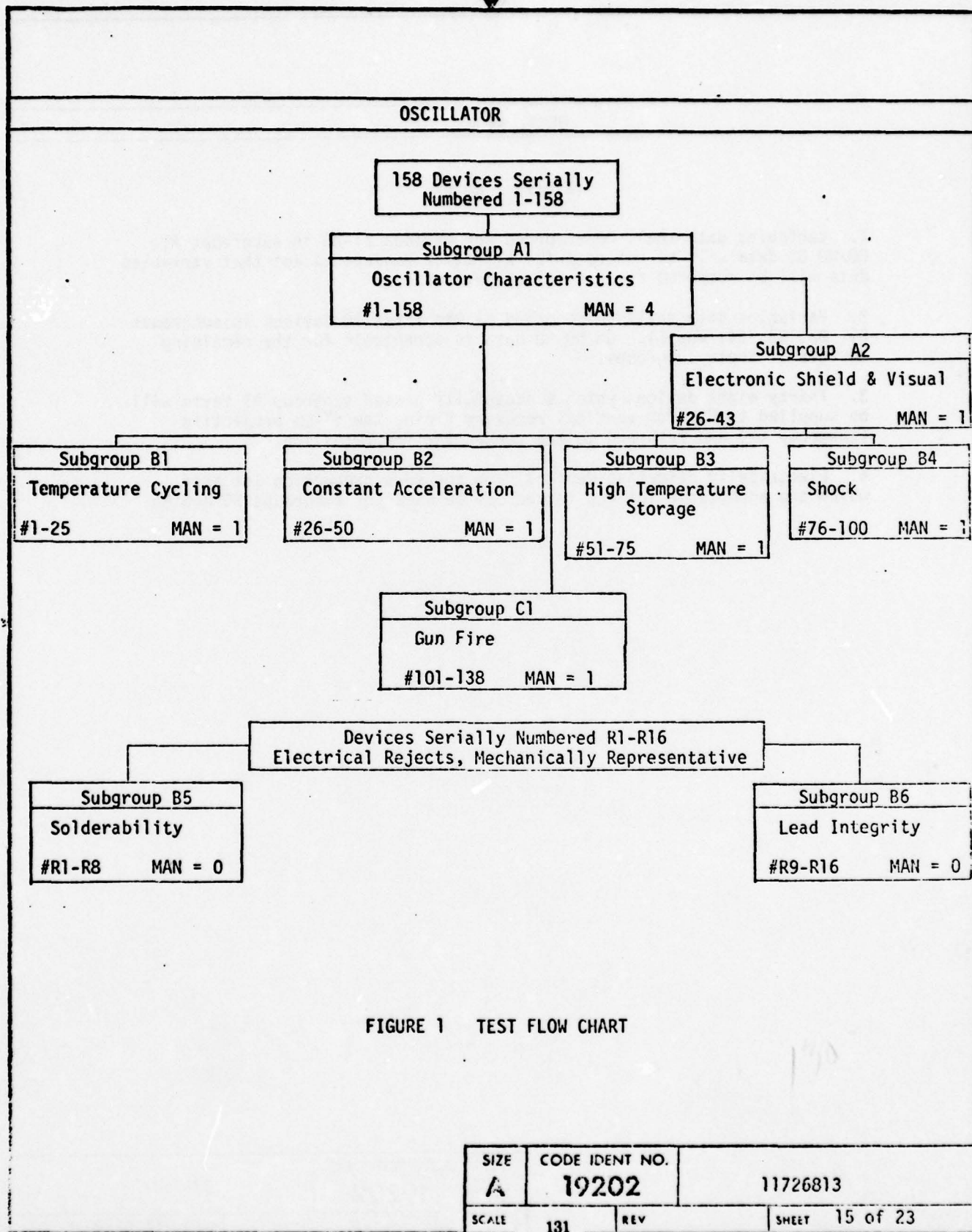


FIGURE 1 TEST FLOW CHART

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Figure 1 Notes

1. Variables data shall be recorded for devices #1-25 in subgroups A1. GO/NO GO data will be recorded for all other devices except that variables data will be recorded for all failed devices.
2. Variables data shall be recorded on the first 10 devices in subgroups B1, B2, B3, B4, and C1. GO/NO GO data is acceptable for the remaining devices in these subgroups.
3. Thirty eight devices which successfully passed subgroup A1 tests will be supplied to HDL for vertical recovery firing the 57-mm projectile (Subgroup C1) and returned to the contractor for retesting.
4. Electrically defective devices from the same production lot from which the acceptable lot was formed may be used for subgroups B5 and B6.

SIZE A	CODE IDENT NO. 19202	11726813
SCALE 132	REV	SHEET 16 of 23

TABLE 1: GROUP A INSPECTION

EXAMINATION OR TEST	MIL-STD-883 METHOD	CONDITIONS		LTPD	MAX ACC NO	SYMBOL	LIMITS		UNITS
		SPECIFIC CONDITIONS					MAX	MIN	
Subgroup 1 Oscillator Characteristics		T=25 +2°C Period Period at B- = -17.0V Period at B- = -30.0V Rise time Fall time Time High Supply current T=45 +2°C Period T=71 +2°C Period Rise time Fall time Time high Supply current T=0 +2°C Period T= -30 +2°C Period T= -50 +2°C Period Rise time Fall time Time high Supply current		5	4	TA	107.000	96.000	μs
						TJ	TA+.012	TA-.012	μs
						TG	TA+.015	TA-.015	μs
						TRA	3.0		μs
						TFA	3.0		μs
						THA	60.0	35.0	μs
						IA	2.70		mA
						TB	TA+.150	TA-.150	μs
						TC	TA+.350	TA-.350	μs
						TRC	3.0		μs
						TFC	3.0		μs
						THC	60.0	35.0	μs
						IA	2.70		mA
						TD	TA+.190	TA-.190	μs
						TE	TA+.410	TA-.410	μs
						TF	TA+.580	TA-.580	μs
						TRF	3.0		μs
						TFF	3.0		μs
						THF	60.0	35.0	μs
						IA	2.70		mA

SIZE

A

CODE IDENT NO.

19202

11726813

SCALE

133

REV

SHEET 17 of 23

OSCILLATOR

TABLE 1: GROUP A INSPECTION (continued)

EXAMINATION OR TEST	MIL-STD-883 METHOD	SPECIFIC CONDITIONS	LTPD NO	MAX ACC NO	SYMBOL	LIMITS		UNITS
						MAX	MIN	
Subgroup 2			20	1				
Electrostatic Shield Attach- ment		Measure resistance between pin 1 and top of package			R	5		ohms
External Visual	2009	Sheet 23						

SIZE A	CODE IDENT NO. 19202	11726813
SCALE	134	REV
		SHEET 18 of 23

TABLE 2: GROUP B INSPECTION

EXAMINATION OR TEST	CONDITIONS		LTPD	MAX ACC NO	SYMBOL	LIMITS		UNITS
	MIL-STD-883 METHOD	SPECIFIC CONDITIONS				MAX	MIN	
<u>Subgroup 1</u> Temperature Cycling	1010	Period before test Test condition A except step 3 Temp is 71 +2°C and steps 1 and 3 stabilization times 15 minutes, 8 cycles. Period after test	15	1	TT1	107.00	96.000	μs
					TT2	TT1+.250	TT1-.250	μs
<u>Subgroup 2</u> Constant Accel- ration	2001	Period at 0 rps Period at test 12500g's orientation Y1	15	1	TS1 TS2	107.000 TS1+.050	96.000 TS1-.050	μs μs
<u>Subgroup 3</u> High Temperature Storage	1008	Period before test Test condition B Test Duration 500 hrs Period after test	15	1	TT3 TT4	107.000 TT3+.250	96.000 TT3-.250	μs μs
<u>Subgroup 4</u> Shock	2002	Period before test Test condition G one shock in orien- tation Z1 Period after test	15	1	TS3 TS4	107.000 TS3+0.020	96.000 TS3-0.020	μs μs

OSCILLATOR

SIZE
ACODE IDENT NO.
19202

11726813

SCALE

135

REV

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OSCILLATOR

TABLE 2: GROUP B INSPECTION (continued)

EXAMINATION OR TEST	CONDITIONS		LTPD	MAX ACC NO	SYMBOL	LIMITS		UNITS
	MIL-STD-883 METHOD	SPECIFIC CONDITIONS				MAX	MIN	
Subgroup 5 Solderability	2003	Pins 1,2,3,4	30	0				
Subgroup 6 Lead Integrity	2004	Test condition B2 Pins 1,2,3,4	30	0				

SIZE
A

CODE IDENT NO.
19202

11726813

SCALE

136

REV

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TABLE 3: GROUP C INSPECTION

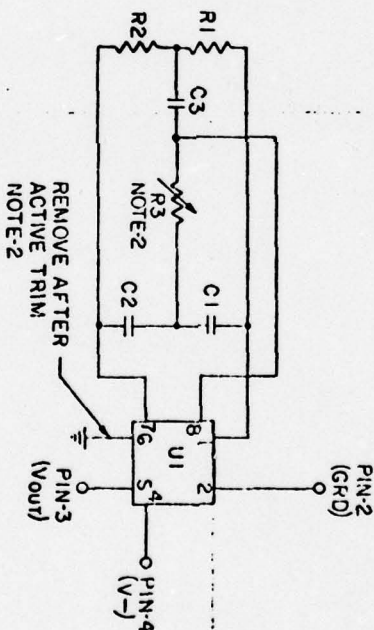
EXAMINATION OR TEST	METHOD	CONDITIONS SPECIFIC CONDITIONS	LTPD NO	MAX ACC NO	SYMBOL	LIMITS		UNITS
						MAX	MIN	
Subgroup 1 Gun Fire		Period before test Government will fire devices in 57-mm gun Period after test	10	1	TGA	107.000	96.000	μs
					TGB	TGA+.050	TGA-0.50	μs

OSCILLATOR

SIZE A	CODE IDENT NO. 19202	11726813
SCALE 137	REV	SHEET 21 of 23

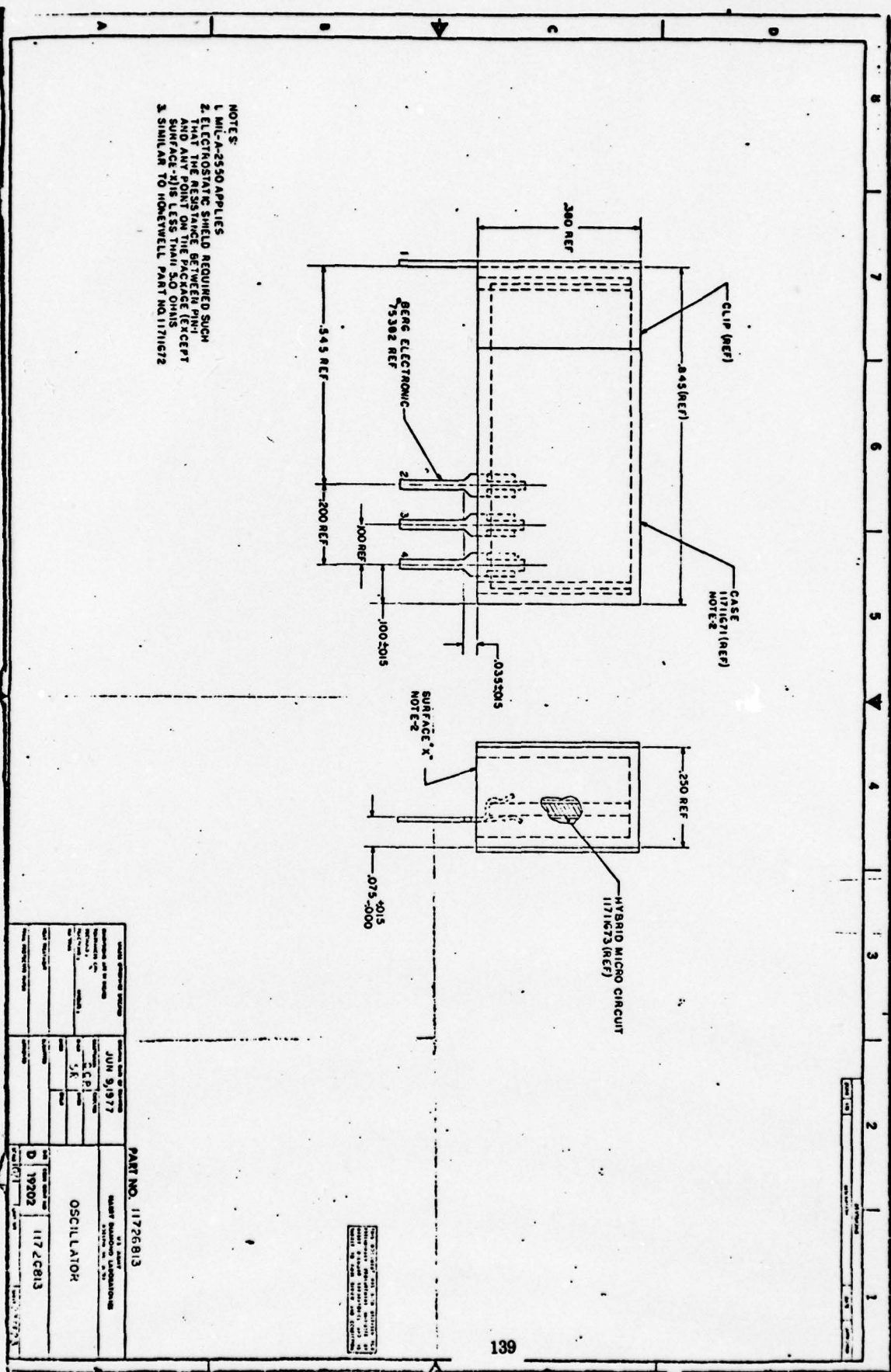
COMPONENT		DESCRIPTION	
1	INTEGRATED CIRCUIT	U1	MONOLITHIC AMPLIFIER
2	CAPACITOR	C1 C2	470 PF $\pm 5\%$ NPO TYPE TCC = 0 ± 30 PPM/ $^{\circ}$ C FROM -55° C TO $+80^{\circ}$ C
3	CAPACITOR	C3	1000 PF $\pm 5\%$ NPO TYPE TCC = 0 ± 30 PPM/ $^{\circ}$ C FROM -55° C TO $+80^{\circ}$ C
4	RESISTOR	R1 R2	34 K $\Omega \pm 1\%$ TCR = 0 ± 25 PPM/ $^{\circ}$ C FROM -55° C TO $+80^{\circ}$ C Pd = 0.6 mW MIN
5	RESISTOR	R3	13.5 K Ω MAX TRIMMABLE TO 13.5 K Ω MIN Pd = 2.0 mW MIN

- NOTES
1. MIL-A-2550 APPLIES
 2. ADVISORY TRIM PROCEDURE:
APPLY -23.5 VOLTS BETWEEN PINS 4
AND 2, INCREASE R3 UNTIL OSCILLATIONS
(AS MEASURED AT PIN-3) STOP, OPEN
CIRCUIT PATH TO PIN-6 OF U1 AFTER TRIM.



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USAFS OPERATING SYMBOL		Original Date of Release		PART NO. 11726813	
DIMENSIONS ARE IN INCHES		JUN 10, 1977		U.S. ARMY	
TOLERANCES ON		DATE		HARRY DIAMOND LABORATORIES	
DIMENSIONS:		CCP		WASHINGTON, D.C. 20315	
FRACTIONS:		INCH		OSCILLATOR SCHEMATIC DIAGRAM	
DECIMALS:		INCH		U.S. ARMY	
NEAT TREATMENT		SUBMITTED		11726813	
FINAL PROTECTIVE PASTE		APPROVED		19202	
		DATE		11726813	
		SCALE		1:1	



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APPENDIX B
TEMPERATURE COEFFICIENT OF PERIOD DATA AND
HISTOGRAMS FOR 210 TAB HMOs FABRICATED
WITH PHASE I MONOLITHIC AMPLIFIER

104 ITEMS

DATA AND HISTOGRAM OF THE TEMPERATURE COEFFICIENT OF THE PERIOD

BETWEEN 25 C AND 71 C. TAB OSCILLATORS WERE

ENCAPSULATED WITH A CONFORMAL COAT BARRIER

LAYER OVER THE SUBSTRATE.

MEAN = 30.23360
ST. DEV. = 4.19955

COEFFICIENT OF SKEWNESS = -.87369

XBAR + 1 SIGMA	34.4331	XBAR - 1 SIGMA	26.0340
XBAR + 2 SIGMA	38.6327	XBAR - 2 SIGMA	21.8345
XBAR + 3 SIGMA	42.8322	XBAR - 3 SIGMA	17.6349

11.14000	27.45000	29.46000	31.65000	33.49000
19.51000	27.48000	29.55000	31.68000	33.72000
20.83000	27.82000	29.64000	31.69000	33.75000
21.59000	28.09000	29.65000	31.70000	33.99000
24.45000	28.12000	29.81000	31.76000	34.03000
24.61000	28.18000	29.87000	31.84000	34.33000
24.77000	28.18000	30.38000	32.03000	34.50000
25.12000	28.21000	30.46000	32.14000	34.52000
25.12000	28.31000	30.46000	32.15000	34.63000
25.13000	28.33000	30.50000	32.18000	34.83000
25.37000	28.39000	30.53000	32.27000	35.18000
26.07000	28.42000	30.79000	32.58000	35.57000
26.10000	28.47000	30.83000	32.63000	35.81000
26.21000	28.48000	30.92000	32.69000	36.44000
26.32000	28.72000	30.97000	32.80000	36.63000
26.66000	28.75000	30.99000	32.92000	36.76000
26.67000	28.82000	31.10000	32.95000	37.43000
26.69000	28.82000	31.12000	33.00000	37.76000
26.97000	28.83000	31.35000	33.09000	38.09000
27.19000	29.03000	31.42000	33.13000	41.24000
27.35000	29.30000	31.59000	33.25000	

DEFINE GRAPH INTERVAL 12
DEFINE LOWER GRAPH LIMIT 10
DEFINE UPPER GRAPH LIMIT 41.5

10.0000 -	12.0000	1	X
12.0000 -	14.0000	0	
14.0000 -	16.0000	0	
16.0000 -	18.0000	0	
18.0000 -	20.0000	1	X
20.0000 -	22.0000	2	XX
22.0000 -	24.0000	0	
24.0000 -	26.0000	7	XXXXXXX
26.0000 -	28.0000	13	XXXXXXXXXXXXX
28.0000 -	30.0000	24	XXXXXXXXXXXXXXXXXXXXX
30.0000 -	32.0000	21	XXXXXXXXXXXXXXXXXXXXX
32.0000 -	34.0000	19	XXXXXXXXXXXXXXXXXXXXX
34.0000 -	36.0000	9	XXXXXXXXXX
36.0000 -	38.0000	5	XXXXXX
38.0000 -	40.0000	1	X
40.0000 -	42.0000	1	X

0 VALUE(S) BELOW LOWER LIMIT
0 VALUE(S) ABOVE UPPER LIMIT

142
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104 ITEMS

DATA AND HISTOGRAM OF THE TEMPERATURE COEFFICIENT OF THE PERIOD
BETWEEN 25 C AND 45 C. TAB OSCILLATORS WERE
ENCAPSULATED WITH A CONFORMAL COAT BARRIER
LAYER OVER THE SUBSTRATE.

MEAN = 32.80440
 ST. DEV. = 4.36646

COEFFICIENT OF SKENNESS = 1.32673

XBAR + 1 SIGMA	37.1709	XBAR - 1 SIGMA	28.4380
XBAR + 2 SIGMA	41.5374	XBAR - 2 SIGMA	24.0715
XBAR + 3 SIGMA	45.9038	XBAR - 3 SIGMA	19.7050

20.44000	30.09000	31.95000	33.85000	36.16000
24.10000	30.14000	32.16000	33.87000	36.20000
24.19000	30.16000	32.18000	33.91000	36.21000
26.18000	30.23000	32.24000	33.92000	36.43000
26.36000	30.32000	32.35000	33.99000	36.75000
26.74000	30.44000	32.38000	33.99000	37.02000
27.17000	30.44000	32.41000	34.06000	37.04000
27.17000	30.56000	32.43000	34.10000	37.09000
27.37000	30.78000	32.49000	34.31000	37.22000
27.59000	30.83000	32.61000	34.34000	37.40000
27.68000	30.96000	32.62000	34.73000	37.43000
28.01000	31.01000	32.79000	34.84000	37.66000
28.17000	31.09000	32.79000	34.90000	37.73000
28.28000	31.10000	33.05000	34.99000	37.77000
28.76000	31.31000	33.14000	35.18000	38.08000
28.90000	31.33000	33.16000	35.25000	38.84000
28.98000	31.34000	33.16000	35.42000	38.91000
29.04000	31.37000	33.54000	35.72000	40.26000
29.12000	31.76000	33.71000	35.73000	40.67000
29.45000	31.85000	33.80000	35.77000	56.98000
29.47000	31.88000	33.81000	36.01000	

DEFINE GRAPH INTERVAL 12
 DEFINE LOWER GRAPH LIMIT 120
 DEFINE UPPER GRAPH LIMIT 157

20.0000 -	22.0000	1	X
22.0000 -	24.0000	0	
24.0000 -	26.0000	2	XX
26.0000 -	28.0000	8	XXXXXXXXXX
28.0000 -	30.0000	10	XXXXXXXXXXXX
30.0000 -	32.0000	22	XXXXXXXXXXXXXXXXXXXXXXXXXXXX
32.0000 -	34.0000	26	XXXXXXXXXXXXXXXXXXXXXXXXXXXX
34.0000 -	36.0000	14	XXXXXXXXXXXXXXXXXXXX
36.0000 -	38.0000	15	XXXXXXXXXXXXXXXXXXXX
38.0000 -	40.0000	3	XXX
40.0000 -	42.0000	2	XX
42.0000 -	44.0000	0	
44.0000 -	46.0000	0	
46.0000 -	48.0000	0	
48.0000 -	50.0000	0	
50.0000 -	52.0000	0	
52.0000 -	54.0000	0	
54.0000 -	56.0000	0	
56.0000 -	58.0000	1	X

0 VALUE(S) BELOW LOWER LIMIT
 0 VALUE(S) ABOVE UPPER LIMIT

104 ITEMS

DATA AND HISTOGRAM OF THE TEMPERATURE COEFFICIENT OF THE PERIOD
 BETWEEN 25 C AND 0 C. TAB OSCILLATORS WERE ENCAPSULATED WITH
 A CONFORMAL COAT BARRIER LAYER OVER THE SUBSTRATE.

MEAN = 35.85520
 ST. DEV. = 5.32260

COEFFICIENT OF SKEWNESS = 2.34081

XBAR + 1 SIGMA	41.1778	XBAR - 1 SIGMA	30.5326
XBAR + 2 SIGMA	46.5004	XBAR - 2 SIGMA	25.2100
XBAR + 3 SIGMA	51.8230	XBAR - 3 SIGMA	19.8874

24.73000	31.95000	34.99000	36.76000	39.56000
25.31000	32.05000	35.00000	36.80000	39.59000
27.69000	32.27000	35.19000	36.91000	39.62000
28.32000	32.32000	35.27000	36.91000	40.05000
28.46000	32.45000	35.37000	37.12000	40.06000
28.62000	32.53000	35.42000	37.26000	40.26000
28.68000	32.96000	35.61000	37.27000	40.39000
28.96000	33.02000	35.66000	37.31000	40.53000
29.50000	33.22000	35.71000	37.37000	40.75000
29.89000	33.56000	35.74000	37.47000	40.81000
30.04000	33.63000	36.02000	37.53000	40.92000
30.59000	33.66000	36.27000	37.54000	41.09000
30.61000	33.92000	36.35000	37.68000	42.10000
30.63000	33.94000	36.49000	37.99000	42.44000
30.75000	33.94000	36.52000	38.00000	42.87000
30.97000	34.14000	36.59000	38.05000	43.48000
31.38000	34.16000	36.63000	38.27000	43.78000
31.72000	34.19000	36.66000	38.43000	44.66000
31.77000	34.66000	36.68000	38.49000	44.84000
31.78000	34.82000	36.70000	38.88000	69.71000
31.85000	34.83000	36.75000	39.30000	

DEFINE GRAPH INTERVAL 12
 DEFINE LOWER GRAPH LIMIT 124
 DEFINE UPPER GRAPH LIMIT 169.9

24.0000 -	26.0000	2	XX
26.0000 -	28.0000	1	X
28.0000 -	30.0000	7	XXXXXXX
30.0000 -	32.0000	12	XXXXXXXXXXXX
32.0000 -	34.0000	14	XXXXXXXXXXXXXX
34.0000 -	36.0000	16	XXXXXXXXXXXXXXXX
36.0000 -	38.0000	25	XXXXXXXXXXXXXXXXXXXXXXXXXXXX
38.0000 -	40.0000	10	XXXXXXXXXX
40.0000 -	42.0000	9	XXXXXXXXXX
42.0000 -	44.0000	5	XXXXXX
44.0000 -	46.0000	2	XX
46.0000 -	48.0000	0	
48.0000 -	50.0000	0	
50.0000 -	52.0000	0	
52.0000 -	54.0000	0	
54.0000 -	56.0000	0	
56.0000 -	58.0000	0	
58.0000 -	60.0000	0	
60.0000 -	62.0000	0	
62.0000 -	64.0000	0	
64.0000 -	66.0000	0	
66.0000 -	68.0000	0	
68.0000 -	70.0000	1	X

0 VALUE(S) BELOW LOWER LIMIT
 0 VALUE(S) ABOVE UPPER LIMIT

ITEMS DATA AND HISTOGRAM OF THE TEMPERATURE COEFFICIENT
 MEAN = 35.80720 BETWEEN 25 C. AND -30 C. TAB OSCILLATORS WERE
 ST. DEV. = 6.59044 ENCAPSULATED WITH A CONFORMAL COAT BARRIER
 OVER THE SUBSTRATE.

COEFFICIENT OF SKEWNESS = -1.21421

XBAR + 1 SIGMA	42.3977	XBAR - 1 SIGMA	29.2168
XBAR + 2 SIGMA	48.9881	XBAR - 2 SIGMA	22.6263
XBAR + 3 SIGMA	55.5786	XBAR - 3 SIGMA	16.0359

14.83000	31.95000	36.34000	38.73000	41.11000
14.89000	32.57000	36.75000	38.92000	41.54000
16.35000	32.62000	36.76000	39.06000	41.66000
18.65000	32.68000	36.77000	39.39000	41.69000
23.06000	33.48000	36.85000	39.69000	41.77000
23.36000	33.73000	37.18000	39.75000	41.86000
23.93000	33.85000	37.31000	39.84000	42.13000
24.02000	34.00000	37.36000	39.89000	42.32000
24.14000	34.21000	37.47000	39.89000	42.41000
25.81000	34.47000	37.49000	39.92000	42.60000
26.90000	34.54000	37.77000	40.10000	42.64000
27.32000	34.73000	38.00000	40.16000	42.76000
28.10000	34.74000	38.21000	40.27000	43.01000
28.37000	35.08000	38.23000	40.30000	43.34000
28.70000	35.18000	38.33000	40.38000	43.81000
28.99000	35.23000	38.40000	40.51000	45.55000
29.81000	35.28000	38.41000	40.56000	49.71000
30.43000	35.48000	38.42000	40.63000	
31.18000	35.65000	38.57000	40.92000	
31.44000	35.78000	38.65000	40.97000	
31.85000	36.32000	38.72000	41.05000	

DEFINE GRAPH INTERVAL 12
 DEFINE LOWER GRAPH LIMIT 14
 DEFINE UPPER GRAPH LIMIT 49.9

14.0000 -	16.0000	2	XX
16.0000 -	18.0000	1	X
18.0000 -	20.0000	1	X
20.0000 -	22.0000	0	
22.0000 -	24.0000	3	XXX
24.0000 -	26.0000	3	XXX
26.0000 -	28.0000	2	XX
28.0000 -	30.0000	5	XXXXX
30.0000 -	32.0000	5	XXXXX
32.0000 -	34.0000	6	XXXXXX
34.0000 -	36.0000	13	XXXXXXXXXXXXXXX
36.0000 -	38.0000	12	XXXXXXXXXXXXXXX
38.0000 -	40.0000	20	XXXXXXXXXXXXXXXXXXXXXXX
40.0000 -	42.0000	17	XXXXXXXXXXXXXXXXXXXXXXX
42.0000 -	44.0000	9	XXXXXXXXXX
44.0000 -	46.0000	1	X
46.0000 -	48.0000	0	
48.0000 -	50.0000	1	X

0 VALUE(S) BELOW LOWER LIMIT
 0 VALUE(S) ABOVE UPPER LIMIT

99 ITEMS DATA AND HISTOGRAM OF THE TEMPERATURE COEFFICIENT OF THE PERIOD

MEAN = 36.13650
ST. DEV. = 6.48262

BETWEEN 25 C AND -50 C. TAB OSCILLATORS WERE
ENCAPSULATED WITH A CONFORMAL COAT BARRIER LAYER
OVER THE SUBSTRATE.

COEFFICIENT OF SKEWNESS = 1.17955

XBAR + 1 SIGMA	42.6191	XBAR - 1 SIGMA	29.6538
XBAR + 2 SIGMA	49.1017	XBAR - 2 SIGMA	23.1712
XBAR + 3 SIGMA	55.5843	XBAR - 3 SIGMA	16.6886

15.28000	32.02000	35.29000	37.25000	39.92000
22.66000	32.07000	35.30000	37.54000	39.94000
25.49000	32.54000	35.30000	37.56000	40.10000
26.17000	32.68000	35.36000	37.61000	40.72000
26.32000	32.73000	35.46000	37.70000	40.84000
26.83000	32.79000	35.61000	37.71000	40.85000
28.40000	33.13000	35.79000	37.86000	40.96000
29.04000	33.27000	35.80000	38.04000	41.09000
29.15000	33.54000	35.82000	38.08000	41.60000
29.18000	33.74000	35.89000	38.15000	41.96000
29.60000	33.94000	36.42000	38.19000	42.02000
30.08000	34.01000	36.46000	38.43000	42.13000
30.16000	34.01000	36.57000	38.65000	42.39000
30.57000	34.34000	36.60000	38.66000	42.52000
30.60000	34.68000	36.64000	38.72000	42.81000
31.06000	34.85000	36.76000	38.89000	44.47000
31.23000	34.88000	36.78000	38.96000	60.22000
31.39000	35.06000	36.78000	39.02000	60.77000
31.50000	35.16000	37.02000	39.04000	62.48000
31.91000	35.25000	37.14000	39.56000	

DEFINE GRAPH INTERVAL 12
DEFINE LOWER GRAPH LIMIT 114
DEFINE UPPER GRAPH LIMIT 163

14.0000 -	16.0000	1	X
16.0000 -	18.0000	0	
18.0000 -	20.0000	0	
20.0000 -	22.0000	0	
22.0000 -	24.0000	1	X
24.0000 -	26.0000	1	X
26.0000 -	28.0000	3	XXX
28.0000 -	30.0000	5	XXXXX
30.0000 -	32.0000	9	XXXXXXXXX
32.0000 -	34.0000	11	XXXXXXXXXXXXX
34.0000 -	36.0000	19	XXXXXXXXXXXXXXXXXXXXX
36.0000 -	38.0000	17	XXXXXXXXXXXXXXXXXXXXX
38.0000 -	40.0000	15	XXXXXXXXXXXXXXXXXXXXX
40.0000 -	42.0000	8	XXXXXXXXXX
42.0000 -	44.0000	5	XXXXX
44.0000 -	46.0000	1	X
46.0000 -	48.0000	0	
48.0000 -	50.0000	0	
50.0000 -	52.0000	0	
52.0000 -	54.0000	0	
54.0000 -	56.0000	0	
56.0000 -	58.0000	0	
58.0000 -	60.0000	0	
60.0000 -	62.0000	2	XX
62.0000 -	64.0000	1	X

0 VALUE(S) BELOW LOWER LIMIT
0 VALUE(S) ABOVE UPPER LIMIT

103 ITEMS

MEAN = 50.16620
ST. DEV. = 4.03777

DATA AND HISTOGRAM OF THE TEMPERATURE COEFFICIENT OF THE
PERIOD BETWEEN 25°C AND 71°C. TAB OSCILLATORS WERE
ENCAPSULATED WITH EPOXY ONLY.

COEFFICIENT OF SKEWNESS = -.61127

XBAR + 1 SIGMA	54.2040	XBAR - 1 SIGMA	46.1284
XBAR + 2 SIGMA	58.2417	XBAR - 2 SIGMA	42.0907
XBAR + 3 SIGMA	62.2795	XBAR - 3 SIGMA	38.0529

38.99000	47.21000	49.41000	52.13000	53.65000
39.11000	47.24000	49.58000	52.27000	53.84000
39.76000	47.49000	49.63000	52.34000	53.92000
39.97000	47.50000	49.74000	52.41000	54.01000
40.20000	47.57000	50.13000	52.41000	54.03000
44.06000	47.60000	50.14000	52.42000	54.27000
44.22000	47.76000	50.22000	52.52000	54.28000
44.71000	48.24000	50.34000	52.56000	54.33000
44.90000	48.43000	50.40000	52.59000	54.47000
44.93000	48.60000	50.47000	52.61000	54.83000
45.34000	48.79000	50.55000	52.65000	55.22000
45.52000	48.85000	50.58000	52.69000	55.36000
45.58000	48.94000	50.60000	52.83000	55.36000
45.69000	48.97000	50.95000	52.84000	55.37000
46.00000	49.00000	51.01000	52.93000	55.37000
46.15000	49.05000	51.15000	53.01000	56.07000
46.48000	49.10000	51.18000	53.09000	57.43000
46.53000	49.11000	51.76000	53.22000	58.71000
46.65000	49.21000	51.78000	53.38000	58.93000
46.86000	49.28000	52.05000	53.44000	
47.06000	49.39000	52.09000	53.53000	

DEFINE GRAPH INTERVAL 12
DEFINE LOWER GRAPH LIMIT 138
DEFINE UPPER GRAPH LIMIT 159

38.0000 -	40.0000	4	XXXX
40.0000 -	42.0000	1	X
42.0000 -	44.0000	0	
44.0000 -	46.0000	9	XXXXXXXXXX
46.0000 -	48.0000	14	XXXXXXXXXXXXXXXXXX
48.0000 -	50.0000	18	XXXXXXXXXXXXXXXXXXXXXX
50.0000 -	52.0000	15	XXXXXXXXXXXXXXXXXXXX
52.0000 -	54.0000	26	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
54.0000 -	56.0000	12	XXXXXXXXXXXXXX
56.0000 -	58.0000	2	XX
58.0000 -	60.0000	2	XX

0 VALUE(S) BELOW LOWER LIMIT
0 VALUE(S) ABOVE UPPER LIMIT

03 ITEMS DATA AND HISTOGRAM OF THE TEMPERATURE COEFFICIENT OF THE PERIOD
 BETWEEN +25°C AND +45°C. TAB OSCILLATORS WERE ENCAPSULATED WITH
 EXOXY ONLY.

MEAN = 52.73440
 ST. DEV. = 4.39592

COEFFICIENT OF SKEWNESS = -.03652

XBAR + 1 SIGMA	57.1303	XBAR - 1 SIGMA	48.3385
XBAR + 2 SIGMA	61.5262	XBAR - 2 SIGMA	43.9425
XBAR + 3 SIGMA	65.9221	XBAR - 3 SIGMA	39.5466

40.81000	49.13000	52.29000	53.73000	56.75000
43.70000	49.38000	52.34000	53.83000	56.77000
43.82000	49.39000	52.41000	53.88000	56.80000
44.22000	49.50000	52.44000	54.15000	56.96000
44.88000	49.66000	52.48000	54.32000	56.99000
45.04000	49.78000	52.69000	54.38000	57.10000
46.28000	50.10000	52.75000	54.76000	57.20000
46.42000	50.14000	52.75000	54.93000	57.91000
46.66000	50.21000	52.85000	55.10000	58.09000
46.69000	50.30000	52.88000	55.11000	58.69000
46.76000	50.96000	52.88000	55.16000	58.82000
46.95000	50.98000	52.91000	55.29000	59.24000
47.13000	51.20000	52.92000	55.38000	59.74000
47.82000	51.33000	52.92000	55.45000	60.23000
48.38000	51.35000	53.06000	55.61000	60.92000
48.47000	51.38000	53.28000	55.73000	61.11000
48.49000	51.41000	53.30000	55.92000	61.50000
48.88000	51.46000	53.49000	56.04000	61.60000
48.88000	51.62000	53.60000	56.16000	64.44000
49.01000	51.64000	53.65000	56.52000	
49.05000	51.80000	53.68000	56.70000	

DEFINE GRAPH INTERVAL 1

2
 DEFINE LOWER GRAPH LIMIT 40
 DEFINE UPPER GRAPH LIMIT 64.4

40.0000 -	42.0000	1	X
42.0000 -	44.0000	2	XX
44.0000 -	46.0000	3	XXX
46.0000 -	48.0000	8	XXXXXXXXX
48.0000 -	50.0000	13	XXXXXXXXXXXXXXX
50.0000 -	52.0000	15	XXXXXXXXXXXXXXXXXX
52.0000 -	54.0000	24	XXXXXXXXXXXXXXXXXXXXXXX
54.0000 -	56.0000	14	XXXXXXXXXXXXXXXXXX
56.0000 -	58.0000	12	XXXXXXXXXXXXXXX
58.0000 -	60.0000	5	XXXXXX
60.0000 -	62.0000	5	XXXXXX
62.0000 -	64.0000	0	
64.0000 -	66.0000	1	X

0 VALUE(S) BELOW LOWER LIMIT
 0 VALUE(S) ABOVE UPPER LIMIT

04 ITEMS

**DATA AND HISTOGRAM OF THE TEMPERATURE COEFFICIENT OF THE PERIOD
BETWEEN 25°C and 0°C. TAB OSCILLATORS WERE ENCAPSULATED
WITH EROXY ONLY.**

MEAN = 56.46730
ST. DEV. = 5.02916

COEFFICIENT OF SKEWNESS = -.47157

XBAR + 1 SIGMA	61.4965	XBAR - 1 SIGMA	51.4382
XBAR + 2 SIGMA	66.5257	XBAR - 2 SIGMA	46.4090
XBAR + 3 SIGMA	71.5548	XBAR - 3 SIGMA	41.3798

38.34000	52.69000	55.43000	58.00000	60.78000
43.99000	52.76000	55.51000	58.15000	61.10000
45.59000	53.06000	55.54000	58.51000	61.26000
46.27000	53.08000	55.84000	58.64000	61.37000
46.86000	53.59000	55.84000	59.13000	61.69000
47.29000	53.71000	55.87000	59.18000	61.86000
49.40000	53.86000	56.17000	59.26000	61.98000
49.85000	53.94000	56.20000	59.29000	62.06000
50.50000	53.99000	56.34000	59.35000	62.24000
50.59000	54.13000	56.44000	59.50000	62.42000
50.61000	54.22000	56.46000	59.52000	62.65000
51.18000	54.26000	56.54000	59.57000	62.79000
51.23000	54.29000	56.58000	59.60000	63.09000
51.36000	54.34000	56.85000	59.68000	63.25000
51.36000	54.44000	56.90000	59.95000	63.57000
51.94000	54.62000	57.06000	60.05000	64.07000
51.99000	54.72000	57.18000	60.13000	64.09000
52.04000	54.79000	57.41000	60.28000	66.30000
52.18000	55.17000	57.56000	60.53000	66.45000
52.39000	55.27000	57.65000	60.54000	69.04000
52.63000	55.42000	57.65000	60.72000	

DEFINE GRAPH INTERVAL 12
DEFINE LOWER GRAPH LIMIT 138
DEFINE UPPER GRAPH LIMIT 17469.5

38.0000 -	40.0000	1	X
40.0000 -	42.0000	0	
42.0000 -	44.0000	1	X
44.0000 -	46.0000	1	X
46.0000 -	48.0000	3	XXX
48.0000 -	50.0000	2	XX
50.0000 -	52.0000	9	XXXXXXXXXX
52.0000 -	54.0000	13	XXXXXXXXXXXXXX
54.0000 -	56.0000	18	XXXXXXXXXXXXXXXXXX
56.0000 -	58.0000	15	XXXXXXXXXXXXXXXXXX
58.0000 -	60.0000	15	XXXXXXXXXXXXXXXXXX
60.0000 -	62.0000	13	XXXXXXXXXXXXXX
62.0000 -	64.0000	8	XXXXXXXXXX
64.0000 -	66.0000	2	XX
66.0000 -	68.0000	2	XX
68.0000 -	70.0000	1	X

0 VALUE(S) BELOW LOWER LIMIT
0 VALUE(S) ABOVE UPPER LIMIT

ITEMS DATA AND HISTOGRAM OF THE TEMPERATURE OF COEFFICIENT OF THE
PERIOD BETWEEN 25 C AND -30 C. TAB OSCILLATORS
WERE ENCAPSULATED WITH EPOXY ONLY.

MEAN = 55.70150
ST. DEV. = 4.04615

COEFFICIENT OF SKEWNESS = -.51330

XBAR + 1 SIGMA	59.7476	XBAR - 1 SIGMA	51.6553
XBAR + 2 SIGMA	63.7938	XBAR - 2 SIGMA	47.6092
XBAR + 3 SIGMA	67.8399	XBAR - 3 SIGMA	43.5630

44.43000	52.23000	55.32000	57.19000	59.20000
44.50000	52.33000	55.59000	57.32000	59.25000
46.75000	52.41000	55.63000	57.39000	59.30000
46.84000	52.47000	55.70000	57.42000	59.35000
47.08000	52.94000	55.94000	57.43000	59.55000
49.65000	53.22000	55.99000	57.49000	59.65000
49.80000	53.48000	56.01000	57.56000	59.67000
49.92000	53.58000	56.02000	57.88000	59.74000
50.07000	53.75000	56.06000	57.89000	59.86000
50.15000	53.92000	56.18000	58.22000	60.38000
50.37000	53.97000	56.31000	58.28000	60.57000
50.51000	54.11000	56.42000	58.30000	60.77000
50.53000	54.15000	56.43000	58.36000	60.85000
50.66000	54.44000	56.52000	58.64000	61.07000
50.79000	54.71000	56.56000	58.67000	61.43000
51.04000	55.00000	56.62000	58.75000	62.37000
51.35000	55.05000	56.65000	58.76000	63.06000
51.42000	55.08000	56.79000	59.01000	63.10000
51.52000	55.08000	56.86000	59.01000	63.24000
51.93000	55.20000	56.87000	59.04000	63.53000
52.01000	55.32000	57.13000	59.04000	

DEFINE GRAPH INTERVAL 12
DEFINE LOWER GRAPH LIMIT 44
DEFINE UPPER GRAPH LIMIT 63.9

44.0000 -	46.0000	2	XX
46.0000 -	48.0000	3	XXX
48.0000 -	50.0000	3	XXX
50.0000 -	52.0000	12	XXXXXXXXXXXXXX
52.0000 -	54.0000	12	XXXXXXXXXXXXXX
54.0000 -	56.0000	16	XXXXXXXXXXXXXXXXXX
56.0000 -	58.0000	24	XXXXXXXXXXXXXXXXXXXXXXXXXXXX
58.0000 -	60.0000	21	XXXXXXXXXXXXXXXXXXXXXXX
60.0000 -	62.0000	6	XXXXXX
62.0000 -	64.0000	5	XXXXX

0 VALUE(S) BELOW LOWER LIMIT
0 VALUE(S) ABOVE UPPER LIMIT

TEMS

DATA AND HISTOGRAM OF THE TEMPERATURE COEFFICIENT OF THE PERIOD

BETWEEN 25°C AND -50°C. TAB OSCILLATOR WEL

MEAN = 51.79410
ST. DEVL = 4.94099

ENCAPSULATED WITH EPOXY ONLY.

COEFFICIENT OF SKEWNESS = -.43856

XBAR + 1 SIGMA	56.7351	XBAR - 1 SIGMA	46.8531
XBAR + 2 SIGMA	61.6761	XBAR - 2 SIGMA	41.9122
XBAR + 3 SIGMA	66.6171	XBAR - 3 SIGMA	36.9712

39.13000	47.30000	51.60000	53.97000	56.47000
40.21000	47.49000	51.64000	54.00000	56.54000
41.13000	47.62000	51.68000	54.00000	56.58000
41.40000	48.65000	52.08000	54.03000	56.69000
42.45000	48.99000	52.11000	54.12000	57.28000
42.77000	49.00000	52.52000	54.14000	57.40000
43.20000	49.18000	52.59000	54.25000	57.40000
44.48000	49.33000	52.59000	54.27000	57.46000
44.63000	49.41000	52.64000	54.30000	57.59000
44.71000	49.67000	52.73000	54.46000	57.68000
45.11000	49.89000	52.93000	54.48000	57.82000
45.11000	50.30000	52.94000	54.61000	58.44000
45.35000	50.76000	53.01000	54.65000	58.73000
45.44000	50.95000	53.06000	54.74000	59.79000
45.61000	51.01000	53.11000	55.04000	59.86000
45.93000	51.06000	53.38000	55.11000	60.40000
45.98000	51.24000	53.58000	55.36000	60.47000
46.04000	51.31000	53.68000	55.42000	62.87000
46.10000	51.36000	53.71000	55.55000	
46.16000	51.53000	53.83000	56.10000	
46.65000	51.55000	53.90000	56.43000	

DEFINE GRAPH INTERVAL 12
DEFINE LOWER GRAPH LIMIT 138
DEFINE UPPER GRAPH LIMIT 163

38.0000 -	40.0000	1	X
40.0000 -	42.0000	3	XXX
42.0000 -	44.0000	3	XXX
44.0000 -	46.0000	10	XXXXXXXXXX
46.0000 -	48.0000	7	XXXXXXX
48.0000 -	50.0000	8	XXXXXXXXXX
50.0000 -	52.0000	13	XXXXXXXXXXXXXX
52.0000 -	54.0000	19	XXXXXXXXXXXXXXXXXXXXXX
54.0000 -	56.0000	18	XXXXXXXXXXXXXXXXXXXXXX
56.0000 -	58.0000	13	XXXXXXXXXXXXXX
58.0000 -	60.0000	4	XXXX
60.0000 -	62.0000	2	XX
62.0000 -	64.0000	1	X

0 VALUE(S) BELOW LOWER LIMIT
0 VALUE(S) ABOVE UPPER LIMIT



**APPENDIX C. FAILURE ANALYSIS OF TAB HMOs THAT FAILED
DURING GROUP A AND B TESTING**

Honeywell

DEFENSE SYSTEMS DIVISION

FAILURE ANALYSIS LAB FAILURE ANALYSIS REPORT



DATE 4/21/78	PROJECT XM587	MALFUNCTION/F&A REPORT NUMBER	REPORT NUMBER 69149
PART NAME 10KHZ TAB Hybrid Microcircuit Oscillator	DRAWING/PART NUMBER 11726813	GENERIC PART/NUMBER	
SERIAL NUMBER	MANUFACTURER Honeywell DSD	DATE CODE	

1. BACKGROUND 2. ANALYSIS PROCEDURE 3. CONCLUSIONS 4. RECOMMENDATIONS (OPTIONAL) 5. EQUIPMENT USED (OPTIONAL)

BACKGROUND

Thirteen TAB hybrid microcircuit oscillators were submitted for failure analysis. The TAB hybrid microcircuit oscillators were being exposed to Group A and B tests of HDL Dwg 11726813. Failure test sequence point and failure modes are listed in the following table:

<u>Serial Number</u>	<u>Failure Mode</u>	
79	No output	Group A, Electrical
294	No output	Group A, Electrical
227	Voltage sensitivity @ -23.5 Vdc to -17 Vdc	Group A, Electrical
5	Voltage sensitivity @ -23.5 Vdc to -17 Vdc	Group A, Electrical
83	Voltage sensitivity @ -23.5 Vdc to -17 Vdc	Group A, Electrical
215	No output @ -20°C and -50°C	Group A, Electrical
95	Period < 96×10^{-6} second 3	Group A, Electrical
298	Period < 96×10^{-6} second 3	Group A, Electrical
35	Supply current > 2.7 mAdc	Group A, Electrical
28	Excessive period drift $T = -552 \times 10^{-9}$	Group B, Moisture Res.
230	Excessive period drift $T = -234.5 \times 10^{-9}$	Group B, Moisture Res.
18	Excessive period drift $T = 279 \times 10^{-9}$	Group B, Temp. Cycle
103	Excessive period drift $T = 619.5 \times 10^{-9}$	Group B, High Temp. Storage

ANALYSIS PROCEDURE

Detailed failure analysis procedures are listed for each TAB hybrid microcircuit oscillator individually.

SN79 (No Output)

Electrical testing showed the device supply current was 455 mAdc. Typical supply current is 2.0 mAdc. After decapsulation, visual examination did not reveal obvious defects. Additional electrical testing was not performed as the Al metallization on the monolithic amplifier was damaged during decapsulation. A defective amplifier was considered the most probable cause of this failure.

SN294 (No Output)

Electrical testing showed the device supply current was 46 mAdc and output latched up at -15 Vdc. After decapsulation, electrical measurements showed the voltage regulator voltage was 15 Vdc and the zener reference voltage was 13.83 Vdc. The zener reference voltage was normal which indicates that the PNP transistor in the voltage regulator circuit was defective. Visual examination did not reveal a defect in this area on the monolithic integrated circuits.

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SN227, 5, and 83 (Voltage Sensitivity @ -23.5 Vdc to -17.0 Vdc)

Electrical testing showed period changes greater than 15×10^{-9} seconds when varying the supply voltage from -23.5 Vdc to -17 Vdc (i.e. SN227, $\Delta T = 36.7 \times 10^{-9}$ seconds; SN5, $\Delta T = 20 \times 10^{-9}$ seconds; SN83, $\Delta T = 27.5 \times 10^{-9}$ seconds). After decapsulation, electrical measurements (monitoring the zener reference voltage and the voltage regulator voltage while varying the supply voltage) were performed to define the relationship between the period change and the reference voltage. Reference Table I. Two hybrid microcircuit oscillators (SN306 & 303) which functioned normally were also included in the testing. The data revealed a greater change in the reference voltage with supply voltages from -23.5 Vdc to -17.0 Vdc when compared to supply voltage from -23.5 Vdc to -30 Vdc. A comparison between the devices that functioned normally and the devices that failed the voltage sensitivity test showed the reference voltage changed approximately 50% of that noted in the defect devices. The zener section of the monolithic amplifier was then isolated by cutting the metal tracks. Electrical microprobe testing was performed to further analyze the isolated zener section. Voltage and current measurements revealed the zener impedance was considerably higher at lower currents on the device which failed the voltage sensitivity tests. It appears the failures resulted from an excessive change in the reference voltage.

SN215 (No Output @ -30°C and -50°C)

The device functioned properly at room temperature. The no output condition at temperature was verified. However, in the failed state, the supply current increased from 1.89 mAdc to 3.25 mAdc. After decapsulation, visual examination did not reveal any defects. The voltage regulator section of the monolithic integrated circuit functioned properly at room temperature. It appears the no output condition at -30°C and -50°C resulted from a defective monolithic amplifier.

SN95 and 298 (Period < 96×10^{-6} Second)

Electrical measurements verified the period of SN95 and SN298 were 95.003×10^{-6} seconds and 95.329×10^{-6} seconds, respectively. A data search revealed that the periods of SN95 and SN298 were low and out of specification limits prior to encapsulation. The devices should have been screened before submitting to the Group A testing.

SN35 (Supply Current > 2.7 mAdc)

Electrical measurements verified the supply current was 9.8 mAdc. A data search revealed that the supply current of device SN35 was high and exceeded the specification limits prior to encapsulation. The device should have been screened before submitting to the Group A testing.

SN28 (Excessive period drift during moisture resistance testing)

A period drift of -552×10^{-9} seconds was noted during the 10 day moisture test (MIL-STD-883, Method 1004.1). This test is not specified in HDL Dwg 11726813. However, the drift rate noted was abnormal. After decapsulation, visual examination revealed flaking, crazing and cracking of the resistor thick film elements. No anomalies were found associated with the capacitors. It appears that this excessive period drift is attributable to resistance changes of the thick film resistors in the Twin-T network due to mechanical stresses from the epoxy encapsulant. Reference Photo #1 and #2.

SN18 (Excessive period drift during temperature cycle, (+71°C to -55°C)

A period drift of 279×10^{-9} seconds was noted after 8 cycles from +71°C to -55°C. Visual examination revealed flaking, crazing, and cracking of the resistor thick film elements. There were no anomalies found associated with the capacitors. The cause of this failure is similar to that of SN28. Reference Photos #1 and #2.

SN103 (Excessive period drift during high temperature storage, 500 hrs @ 125°C)

A period drift of 619.5×10^{-9} seconds was noted after 500 hrs. @ 125°C. Visual examination showed flaking, crazing, and cracking of the resistor thick film elements. There were no anomalies found associated with the capacitors. The cause of this failure is similar to that of SN28 above. Reference Photo #1 and #2.

SN230 (Excessive period drift during moisture resistance)

A period drift of -234.5×10^{-9} was noted during the 10 day moisture resistance test (MIL-STD-883, Method 1004.1). This test is not specified in HDL Dwg. 11726813. However, the period drift was considerably greater than that noted for the other test samples which were exposed to this test. After decapsulation, visual examination did not reveal any defects. Electrical measurements of the resistor and capacitor values were within the specified requirements. Minor drifts in the resistance and/or capacitance of the Twin-T network elements are the most probable cause of this failure.

CONCLUSIONS

The failures can be summarized in four major areas:

- 1) Devices SN79 and 294 failed due to defective monolithic amplifiers.
- 2) Devices SN5, 83, and 227 failed due to excessive changes in the reference voltage when varying the supply voltage from -23.5 Vdc to -17.0 Vdc. The excessive reference voltage is due to higher zener impedance at low current levels.
- 3) Device SN95, 298, and 35 failed Group A testing. However, these devices should have been screened by electrical testing after encapsulation prior to Group A testing.
- 4) Devices SN28, 230, 18 and 103 failed due to minor drifts (i.e. $\approx 0.25\%$ can cause an out of specification condition) of the resistors and/or capacitors of the Twin-T network. Minor resistance and capacitance changes are undetectable without knowledge of the initial value.

Prepared by

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J.A. Roth
Failure Analyst

Approved by

D.A. Tabor
D.A. Tabor
Reliability Engineer

TABLE I
ELECTRICAL DATA OF VOLTAGE
REGULATOR SECTION

Device S/N	Supply Voltage (Vdc)	τ (10^{-6} sec.)	ΔT (10^{-9} sec.)	V_{reg} (mVdc)	ΔV_{reg} (mVdc)	V_{Σ} (Vdc)	ΔV_{Σ} (mVdc)	I_s (mA)	ΔI_s (μ A)
#303 (Good)	-17	98.6459	4.5	12.361	67	13.023	60	1.882	132
	-23.5	98.6414		12.428		13.083		2.014	
	-30	98.6305	10.9	12.486	58	13.141	58	2.143	129
	-35	98.6308	10.6	12.546	118	13.193	110	2.244	230
	-40	98.6271	14.3	12.593	165	13.240	157	2.343	329
	-45	98.6269	14.5	12.647	219	13.292	209	2.440	426
#306 (Good)	-17	96.2648	4.5	12.457	67	13.116	62	1.869	131
	-23.5	96.2603		12.524		13.178		2.000	
	-30	96.2516	8.7	12.591	67	13.243	65	2.128	128
	-35	96.2522	8.1	12.645	121	13.293	115	2.223	223
	-40	95.2465	13.8	12.689	165	13.332	154	2.318	318
	-45	96.2470	13.3	12.736	212	13.377	199	2.411	411
#227 (Failed)	-17	98.9774	36.7	12.452	96	13.074	133	1.578	122
	-23.5	98.9407		12.548		13.207		1.700	
	-30	98.9294	11.3	12.612	64	13.262	55	1.815	115
	-35	98.9285	12.2	12.645	97	13.293	86	1.896	196
	-40	98.9235	17.2	12.672	124	13.319	112	1.980	280
	-45	98.9222	18.5	12.706	158	13.348	141	2.061	361
#5 (Failed)	-17	96.4060	20	12.219	224	12.878	97	1.591	229
	-23.5	96.3860		12.443		13.098		1.820	
	-30	96.3760	10	12.545	102	13.197	99	2.027	207
	-35	96.3651	20.9	17.593	150	13.252	154	2.183	363
	-40	96.3672	18.8	12.658	215	13.303	205	2.335	515
	-45	96.3673	18.7	12.702	259	13.346	248	2.484	664
#83 (Failed)	-17	97.9932	27.5	12.424	102	13.087	98	1.902	220
	-23.5	97.9657		12.526		13.185		2.122	
	-30	97.9612	4.5	12.597	71	13.252	67	2.282	160
	-35	97.9539	11.8	12.630	104	13.286	101	2.394	272
	-40	97.8761	89.6	12.675	149	13.325	140	2.784	662
	-45	97.9033	62.4	12.747	221	13.375	190	4.450	2,328

Note all delta measurements taken with respect to -23.5 Vdc.

HARD EPOXY ENCAPSULATED UNIT #18



Photo #1 (Unit #18)

Magnification 8.75X

Photo shows the damaged area of R1 and R2 film.

Note: Large chip out. The resistive film was bonded to the glass. The chip came loose during decapsulation.

The area under the marker C is loose from the substrate. The point of the marker indicates the start of the crack.

The arrow shows where the crack ends.

HARD EPOXY ENCAPSULATED UNIT #18

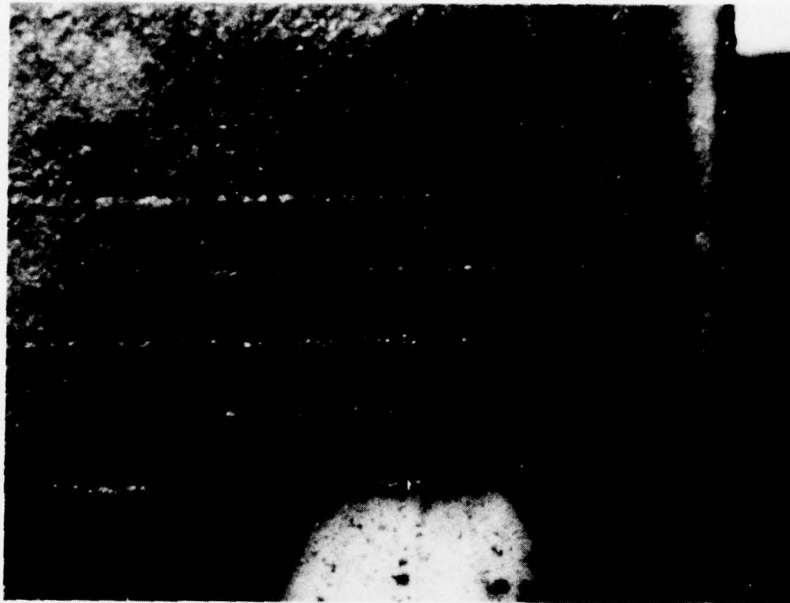


Photo #2 (Unit #18)

Magnification 30X

Enlargement of the damaged area as indicated by the arrow and marker in photo #1.

APPENDIX D
FAILURE ANALYSIS OF TAB HMOs AFTER 57-mm TESTING

Honeywell

DEFENSE SYSTEMS DIVISION

FAILURE ANALYSIS LAB FAILURE ANALYSIS REPORT



DATE 5/17/78	PROJECT XM587	MALFUNCTION/F&A REPORT NUMBER	REPORT NUMBER 69299
PART NAME 10KHZ Hybrid Microcircuit Oscillator	DRAWING/PART NUMBER 11726813	GENERIC PART/NUMBER	
SERIAL NUMBER	MANUFACTURER Honeywell DSD	DATE CODE	

1. BACKGROUND

2. ANALYSIS PROCEDURE

3. CONCLUSIONS

4. RECOMMENDATIONS
(OPTIONAL)

5. EQUIPMENT USED
(OPTIONAL)

BACKGROUND

Five Tape Automatic Bonded (TAB) hybrid microcircuit oscillators were submitted for failure analysis after 57MM testing per HDL Dwg 11726813, Group C inspection (Subgroup 1). Three of the five failures exhibited period (T) drifts which exceeded the $\pm 50 \times 10^{-9}$ second specification requirement. The other two failures did not oscillate (i.e. the output latched up at approximately -12.4 Vdc).

ANALYSIS

Electrical measurements are shown in Table I.

TABLE I
ELECTRICAL MEASUREMENTS

SERIAL NUMBER	T PRE-SHOCK (10^{-6} sec)	T POST SHOCK (10^{-6} sec)	ΔT PRE-POST (10^{-6} sec)	T FA LAB (10^{-6} sec)	I_s (mA dc)	ENCAPSULATION TECHNIQUE
41	100.4117	100.4964	.0847	100.3983	1.94	Epoxy
51	98.6918	226.6093	127.9	222.8250	2.06	Epoxy
61	96.9168	245.1698	148.3	229.2600	2.01	Epoxy
71	97.6763	-12.6Vdc	---	-12.4Vdc	1.78	Epoxy
243	97.0255	-12.4Vdc	---	-12.4Vdc	2.04	Silicone barrier layer & epoxy

The electrical measurements performed during failure analysis verified the reported failure modes. All current measurements appear to be normal which is indicative of the monolithic amplifier functioning properly.

Four of the five TAB hybrid microcircuit oscillator failures (SN 41, 51, 61 and 71) were encapsulated with epoxy and one of the TAB hybrid microcircuit oscillator failures (SN 243) was encapsulated with a silicone barrier layer over the entire substrate.

After partial decapsulation of devices, (SN51, SN61, and SN71) resistance measurements of R1 and R2 revealed resistance values considerably greater than the nominal value of $34k\Omega$. R2 in device SN71 was open. After complete decapsulation visual examination revealed large cracks in the thick film dielectric and thick film resistive elements of R1 and R2. The excessive

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period drift in devices SN51 and SN61 and no output condition of SN71 were due to cracks in the thick film resistive elements of R1 and/or R2.

After decapsulation of device SN41, electrical measurements revealed the component values of the R&C elements in the Twin-T network were very close to the nominal values. Visual examination revealed slight evidence of physical damage (cracking) in the lower corner of the R2 resistive film. Minor changes in resistance which are undetectable because the initial values of the components are unknown. This could result in a failure mode of this type.

Electrical measurements of the R and C elements in the Twin-T network of device SN243, revealed R3 had a higher resistance value ($R3 = 16.3k\Omega$) than typically noted. A resistor was placed in parallel with R3, decreasing the value of R3 in the Twin-T network to approximately $15.5k\Omega$. This allowed the oscillator to function properly. Visual examination of R3 did not reveal any defects.

CONCLUSION

Electrical measurements verified 3 of the 5 TAB hybrid microcircuit oscillators failed due to excessive period drifts and 2 of 5 TAB hybrid microcircuit oscillators failed because the output was latched up at -12.4Vdc.

The excessive period drift of devices SN51 and SN61 was due to cracks in the thick film resistive elements of R1 and/or R2. Device SN71 failed due to an open resistor, R2. Visual examination revealed cracks in the thick film elements of R1 and R2. Devices SN51, SN61 and SN71 were encapsulated with epoxy only.

The period drift which device SN41 exhibited was apparently due to minor drift in the R and/or C elements of the Twin-T network. These minor drifts are undetectable as the initial component values were unknown. Minor drifts in the R and/or C elements of the Twin-T network within their specified tolerances would cause this type of failure.

Device SN243 failed due to R3 increasing in resistance. R3 was $16.3k\Omega$ whereas it typically measures approximately $15.5k\Omega$. No visual defects were noted in R3.

Prepared by

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Failure Analyst

Approved by

D. A. Tabor
D. A. Tabor
Reliability Engineer

FAILURE ANALYSIS REPORT

Report Number 69299

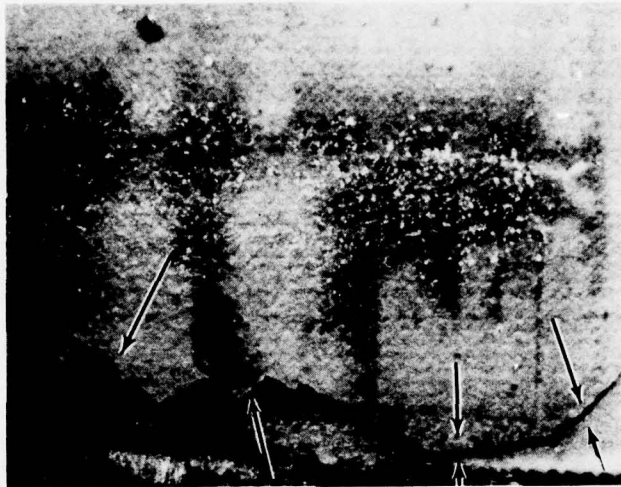


Photo of Unit #51

Magnification 16X

The arrows on this photo show the extent of cracking.

Note the damage is predominantly associated with the film resistor R2 located to the right of the photo.

APPENDIX E
TEMPERATURE COEFFICIENT OF PERIOD DATA AND
HISTOGRAMS FOR 180 TAB HMOs FABRICATED
WITH PHASE II MONOLITHIC AMPLIFIER

175 ITEMS

DATA AND GRAPH OF THE TEMPERATURE COEFFICIENT OF THE PERIOD BETWEEN 25°C and 45°C ppm/°C

MEAN = 30.52730
ST. DEV. = 5.28975

COEFFICIENT OF SKENNESS = 2.27368

XBAR + 1 SIGMA	35.8170	XBAR - 1 SIGMA	25.2375
XBAR + 2 SIGMA	41.1068	XBAR - 2 SIGMA	19.9478
XBAR + 3 SIGMA	46.3965	XBAR - 3 SIGMA	14.6580

18.11000	26.70000	29.49000	31.47000	33.80000
18.28000	26.78000	29.54000	31.58000	33.81000
20.27000	26.82000	29.64000	31.68000	33.87000
21.02000	26.83000	29.69000	31.71000	33.91000
21.35000	26.84000	29.73000	31.73000	33.96000
21.72000	27.02000	29.76000	31.86000	34.04000
22.28000	27.06000	29.76000	31.87000	34.20000
22.34000	27.23000	29.78000	31.92000	34.75000
23.22000	27.24000	29.84000	32.05000	34.90000
23.26000	27.25000	29.87000	32.09000	34.92000
23.34000	27.48000	29.93000	32.17000	35.26000
24.14000	27.52000	29.96000	32.20000	35.39000
24.15000	27.56000	29.97000	32.21000	35.45000
24.33000	27.80000	29.97000	32.29000	35.69000
24.55000	27.89000	30.01000	32.42000	35.86000
24.56000	27.93000	30.06000	32.51000	35.87000
24.72000	27.96000	30.31000	32.57000	36.15000
24.84000	28.02000	30.41000	32.65000	36.15000
25.04000	28.17000	30.62000	32.75000	36.23000
25.13000	28.23000	30.71000	32.76000	36.23000
25.13000	28.37000	30.80000	32.99000	36.35000
25.18000	28.39000	30.82000	33.08000	36.46000
25.70000	28.51000	30.83000	33.10000	36.64000
25.78000	28.51000	30.89000	33.38000	36.88000
25.79000	28.75000	30.90000	33.39000	37.09000
25.79000	28.93000	30.91000	33.50000	37.25000
25.91000	28.95000	30.92000	33.51000	37.60000
26.10000	28.97000	30.96000	33.51000	37.85000
26.15000	29.02000	31.00000	33.54000	38.45000
26.20000	29.03000	31.01000	33.55000	38.49000
26.28000	29.06000	31.09000	33.62000	38.53000
26.34000	29.09000	31.25000	33.68000	38.85000
26.48000	29.30000	31.27000	33.70000	39.57000
26.49000	29.34000	31.44000	33.72000	44.24000
26.53000	29.38000	31.46000	33.75000	70.04000

DEFINE GRAPH INTERVAL !1.0
DEFINE LOWER GRAPH LIMIT !18.0
DEFINE UPPER GRAPH LIMIT !71.0

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18.0000 -	19.0000	2	XX	DATA AND HISTOGRAM....25°C and 45°C ppm/°C (continued)
19.0000 -	20.0000	0		
20.0000 -	21.0000	1	X	
21.0000 -	22.0000	3	XXX	
22.0000 -	23.0000	2	XX	
23.0000 -	24.0000	3	XXX	
24.0000 -	25.0000	7	XXXXXXX	
25.0000 -	26.0000	9	XXXXXXXXX	
26.0000 -	27.0000	13	XXXXXXXXXXXXX	
27.0000 -	28.0000	12	XXXXXXXXXXXXX	
28.0000 -	29.0000	11	XXXXXXXXXXXXX	
29.0000 -	30.0000	21	XXXXXXXXXXXXXXXXXXXXX	
30.0000 -	31.0000	14	XXXXXXXXXXXXXXX	
31.0000 -	32.0000	15	XXXXXXXXXXXXXXXXXX	
32.0000 -	33.0000	13	XXXXXXXXXXXXXXX	
33.0000 -	34.0000	19	XXXXXXXXXXXXXXXXXXXXX	
34.0000 -	35.0000	5	XXXXXX	
35.0000 -	36.0000	6	XXXXXXX	
36.0000 -	37.0000	8	XXXXXXXXXX	
37.0000 -	38.0000	4	XXXXX	
38.0000 -	39.0000	4	XXXXX	
39.0000 -	40.0000	1	X	
40.0000 -	41.0000	0		
41.0000 -	42.0000	0		
42.0000 -	43.0000	0		
43.0000 -	44.0000	0		
44.0000 -	45.0000	1	X	
45.0000 -	46.0000	0		
46.0000 -	47.0000	0		
47.0000 -	48.0000	0		
48.0000 -	49.0000	0		
49.0000 -	50.0000	0		
50.0000 -	51.0000	0		
51.0000 -	52.0000	0		
52.0000 -	53.0000	0		
53.0000 -	54.0000	0		
54.0000 -	55.0000	0		
55.0000 -	56.0000	0		
56.0000 -	57.0000	0		
57.0000 -	58.0000	0		
58.0000 -	59.0000	0		
59.0000 -	60.0000	0		
60.0000 -	61.0000	0		
61.0000 -	62.0000	0		
62.0000 -	63.0000	0		
63.0000 -	64.0000	0		
64.0000 -	65.0000	0		
65.0000 -	66.0000	0		
66.0000 -	67.0000	0		
67.0000 -	68.0000	0		
68.0000 -	69.0000	0		
69.0000 -	70.0000	0		
70.0000 -	71.0000	1	X	
71.0000 -	72.0000	0		

0 VALUE(S) BELOW LOWER LIMIT
0 VALUE(S) ABOVE UPPER LIMIT

DEFINE GRAPH INTERVAL 10

175 ITEMS

175 ITEMS

MEAN = 31.83690
ST. DEV. = 4.07215

**DATA AND HISTOGRAM OF THE TEMPERATURE
COEFFICIENT OF THE PERIOD BETWEEN
25 C to 71 C ppm/ C**

COEFFICIENT OF SKEWNESS = -.30332

XBAR + 1 SIGMA	35.9090	XBAR - 1 SIGMA	27.7647
XBAR + 2 SIGMA	39.9812	XBAR - 2 SIGMA	23.6925
XBAR + 3 SIGMA	44.0533	XBAR - 3 SIGMA	19.6204

16.79000	28.87000	30.78000	32.89000	35.14000
20.24000	29.12000	30.85000	32.92000	35.16000
21.08000	29.14000	30.99000	32.96000	35.17000
21.73000	29.15000	31.07000	33.17000	35.22000
23.30000	29.50000	31.09000	33.25000	35.38000
23.84000	29.51000	31.10000	33.32000	35.39000
24.62000	29.54000	31.29000	33.33000	35.47000
24.95000	29.58000	31.33000	33.39000	35.63000
25.02000	29.62000	31.46000	33.39000	35.73000
25.21000	29.64000	31.46000	33.39000	35.74000
25.65000	29.64000	31.48000	33.46000	35.77000
26.04000	29.68000	31.50000	33.46000	35.81000
26.18000	29.68000	31.51000	33.60000	36.08000
26.35000	29.72000	31.52000	33.70000	36.33000
26.54000	29.82000	31.57000	33.78000	36.34000
26.93000	29.84000	31.60000	33.82000	36.65000
27.03000	29.87000	31.61000	33.90000	36.86000
27.04000	29.89000	31.61000	34.07000	36.89000
27.28000	29.90000	31.96000	34.12000	36.89000
27.36000	29.92000	31.99000	34.12000	37.02000
27.39000	30.00000	32.04000	34.14000	37.09000
27.84000	30.03000	32.06000	34.27000	37.27000
27.85000	30.05000	32.12000	34.27000	37.33000
27.92000	30.14000	32.40000	34.30000	37.50000
27.95000	30.23000	32.42000	34.31000	37.67000
28.12000	30.23000	32.44000	34.31000	37.96000
28.15000	30.28000	32.46000	34.40000	37.98000
28.15000	30.31000	32.58000	34.49000	38.73000
28.18000	30.47000	32.59000	34.63000	39.24000
28.22000	30.58000	32.59000	34.63000	39.67000
28.28000	30.59000	32.68000	34.63000	40.82000
28.29000	30.61000	32.75000	34.66000	41.01000
28.29000	30.65000	32.82000	34.88000	41.20000
28.71000	30.70000	32.87000	34.91000	41.51000
28.85000	30.76000	32.88000	34.93000	41.90000

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DEFINE GRAPH INTERVAL 11.0 DATA AND HISTOGRAM...
 DEFINE LOWER GRAPH LIMIT 116.0 25 C to 71 C ppm/ C
 DEFINE UPPER GRAPH LIMIT 142.0 (continued)

16.0000 -	17.0000	1	X
17.0000 -	18.0000	0	
18.0000 -	19.0000	0	
19.0000 -	20.0000	0	
20.0000 -	21.0000	1	X
21.0000 -	22.0000	2	XX
22.0000 -	23.0000	0	
23.0000 -	24.0000	2	XX
24.0000 -	25.0000	2	XX
25.0000 -	26.0000	3	XXX
26.0000 -	27.0000	5	XXXXX
27.0000 -	28.0000	9	XXXXXXXXX
28.0000 -	29.0000	11	XXXXXXXXXXXX
29.0000 -	30.0000	19	XXXXXXXXXXXXXXXXXXXX
30.0000 -	31.0000	18	XXXXXXXXXXXXXXXXXXXX
31.0000 -	32.0000	17	XXXXXXXXXXXXXXXXXXXX
32.0000 -	33.0000	18	XXXXXXXXXXXXXXXXXXXX
33.0000 -	34.0000	14	XXXXXXXXXXXXXXXXXXXX
34.0000 -	35.0000	18	XXXXXXXXXXXXXXXXXXXX
35.0000 -	36.0000	12	XXXXXXXXXXXX
36.0000 -	37.0000	7	XXXXXXX
37.0000 -	38.0000	8	XXXXXXXXX
38.0000 -	39.0000	1	X
39.0000 -	40.0000	2	XX
40.0000 -	41.0000	1	X
41.0000 -	42.0000	4	XXXX
42.0000 -	43.0000	0	

0 VALUE(S) BELOW LOWER LIMIT
 0 VALUE(S) ABOVE UPPER LIMIT

DEFINE GRAPH INTERVAL 10

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175 ITEMS

MEAN = 37.76970
ST. DEV. = 4.85201

DATA AND HISTOGRAM OF THE TEMPERATURE
COEFFICIENT OF THE PERIOD BETWEEN
25 C to 0 C ppm/ C

COEFFICIENT OF SKEWNESS = -.01286

XBAR + 1 SIGMA	42.6217	XBAR - 1 SIGMA	32.9176
XBAR + 2 SIGMA	47.4737	XBAR - 2 SIGMA	28.0656
XBAR + 3 SIGMA	52.3257	XBAR - 3 SIGMA	23.2136

24.81000	34.07000	36.68000	39.36000	41.33000
25.98000	34.07000	36.70000	39.52000	41.47000
27.37000	34.08000	36.75000	39.61000	41.64000
27.45000	34.10000	36.77000	39.63000	41.66000
27.65000	34.21000	36.79000	39.63000	41.81000
27.68000	34.56000	36.85000	39.66000	42.12000
27.80000	34.62000	36.86000	39.72000	42.24000
28.62000	34.70000	36.87000	39.73000	42.52000
29.17000	34.74000	36.88000	39.74000	42.58000
29.19000	34.76000	37.14000	39.74000	42.78000
30.13000	34.78000	37.19000	39.78000	42.86000
30.45000	34.83000	37.20000	39.81000	42.95000
30.47000	34.87000	37.26000	39.82000	43.01000
30.77000	35.03000	37.27000	39.83000	43.15000
31.30000	35.18000	37.35000	39.96000	43.36000
31.45000	35.35000	37.38000	39.97000	43.41000
31.51000	35.38000	37.53000	39.98000	43.69000
31.56000	35.38000	37.56000	40.02000	43.73000
31.59000	35.46000	37.96000	40.03000	43.89000
31.70000	35.49000	38.10000	40.07000	44.06000
32.06000	35.72000	38.16000	40.10000	44.48000
32.56000	35.80000	38.20000	40.13000	44.73000
32.68000	35.83000	38.21000	40.18000	45.14000
32.71000	35.84000	38.26000	40.36000	45.49000
32.79000	35.88000	38.33000	40.41000	45.93000
32.95000	35.96000	38.36000	40.45000	46.49000
33.23000	36.07000	38.49000	40.51000	46.91000
33.27000	36.10000	38.64000	40.52000	47.02000
33.28000	36.12000	38.65000	40.77000	47.26000
33.40000	36.28000	38.78000	40.87000	47.26000
33.65000	36.45000	38.86000	40.90000	47.51000
33.82000	36.46000	39.00000	41.06000	48.13000
33.82000	36.53000	39.06000	41.07000	49.15000
33.90000	36.56000	39.19000	41.21000	49.38000
33.95000	36.63000	39.21000	41.30000	50.00000

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DEFINE GRAPH INTERVAL 11.0
 DEFINE LOWER GRAPH LIMIT 24.0
 DEFINE UPPER GRAPH LIMIT 51.0

DATA AND HISTOGRAM...
 25 C to 0 C ppm/ C (continued)

24.0000 -	25.0000	1	X
25.0000 -	26.0000	1	X
26.0000 -	27.0000	0	
27.0000 -	28.0000	5	XXXXX
28.0000 -	29.0000	1	X
29.0000 -	30.0000	2	XX
30.0000 -	31.0000	4	XXXX
31.0000 -	32.0000	6	XXXXXX
32.0000 -	33.0000	6	XXXXXX
33.0000 -	34.0000	9	XXXXXXXXXX
34.0000 -	35.0000	13	XXXXXXXXXXXXXX
35.0000 -	36.0000	13	XXXXXXXXXXXXXX
36.0000 -	37.0000	18	XXXXXXXXXXXXXXXXXX
37.0000 -	38.0000	10	XXXXXXXXXX
38.0000 -	39.0000	12	XXXXXXXXXXXXXX
39.0000 -	40.0000	21	XXXXXXXXXXXXXXXXXXXXXX
40.0000 -	41.0000	14	XXXXXXXXXXXXXX
41.0000 -	42.0000	9	XXXXXXXXXX
42.0000 -	43.0000	7	XXXXXXX
43.0000 -	44.0000	7	XXXXXXX
44.0000 -	45.0000	3	XXX
45.0000 -	46.0000	3	XXX
46.0000 -	47.0000	2	XX
47.0000 -	48.0000	4	XXXX
48.0000 -	49.0000	1	X
49.0000 -	50.0000	2	XX
50.0000 -	51.0000	1	X
51.0000 -	52.0000	0	

0 VALUE(S) BELOW LOWER LIMIT
 0 VALUE(S) ABOVE UPPER LIMIT

DEFINE GRAPH INTERVAL 10

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174 ITEMS

MEAN = 40.90870
ST. DEV. = 5.13249

DATA AND HISTOGRAM OF TEMPERATURE
COEFFICIENT OF THE PERIOD BETWEEN
25 C to -30 C ppm/ C

COEFFICIENT OF SKEWNESS = -1.21467

XBAR + 1 SIGMA	46.0412	XBAR - 1 SIGMA	35.7762
XBAR + 2 SIGMA	51.1737	XBAR - 2 SIGMA	30.6437
XBAR + 3 SIGMA	56.3062	XBAR - 3 SIGMA	25.5112

14.57000	37.33000	40.62000	42.54000	44.72000
21.24000	37.52000	40.67000	42.60000	44.76000
28.61000	37.58000	40.70000	42.60000	44.78000
28.89000	37.78000	40.70000	42.61000	45.20000
30.78000	37.96000	40.73000	42.62000	45.27000
30.95000	38.07000	40.73000	42.75000	45.30000
31.09000	38.15000	40.76000	42.85000	45.34000
31.56000	38.36000	40.83000	42.91000	45.37000
32.12000	38.59000	40.85000	42.93000	45.93000
32.20000	38.61000	40.92000	42.96000	46.21000
32.44000	38.66000	40.92000	43.11000	46.22000
32.52000	38.89000	40.92000	43.12000	46.23000
33.71000	38.98000	41.06000	43.20000	46.23000
34.02000	39.00000	41.09000	43.41000	46.26000
34.17000	39.02000	41.13000	43.45000	46.30000
34.19000	39.03000	41.21000	43.51000	46.95000
34.27000	39.04000	41.44000	43.53000	46.99000
34.98000	39.11000	41.46000	43.55000	47.09000
35.10000	39.24000	41.49000	43.57000	47.22000
35.38000	39.44000	41.53000	43.58000	47.38000
35.75000	39.47000	41.64000	43.71000	47.38000
35.79000	39.48000	41.67000	43.76000	47.40000
35.81000	39.48000	41.68000	43.77000	47.65000
35.96000	39.62000	41.71000	43.85000	47.93000
36.14000	39.66000	41.79000	43.96000	48.36000
36.17000	39.72000	41.80000	44.07000	48.81000
36.35000	39.78000	41.97000	44.13000	48.99000
36.48000	39.86000	42.13000	44.15000	49.23000
36.56000	40.01000	42.14000	44.21000	49.32000
36.89000	40.10000	42.16000	44.31000	49.32000
36.91000	40.16000	42.17000	44.32000	49.34000
36.94000	40.22000	42.23000	44.34000	49.62000
37.01000	40.27000	42.24000	44.62000	50.12000
37.29000	40.37000	42.40000	44.64000	51.81000
37.32000	40.50000	42.43000	44.70000	

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DEFINE GRAPH INTERVAL !1.0
 DEFINE LOWER GRAPH LIMIT !14.0
 DEFINE UPPER GRAPH LIMIT !52.0

DATA AND HISTOGRAM...
 25 C to -30 C ppm/ C
 (continued)

14.0000 -	15.0000	1	X
15.0000 -	16.0000	0	
16.0000 -	17.0000	0	
17.0000 -	18.0000	0	
18.0000 -	19.0000	0	
19.0000 -	20.0000	0	
20.0000 -	21.0000	0	
21.0000 -	22.0000	1	X
22.0000 -	23.0000	0	
23.0000 -	24.0000	0	
24.0000 -	25.0000	0	
25.0000 -	26.0000	0	
26.0000 -	27.0000	0	
27.0000 -	28.0000	0	
28.0000 -	29.0000	2	XX
29.0000 -	30.0000	0	
30.0000 -	31.0000	2	XX
31.0000 -	32.0000	2	XX
32.0000 -	33.0000	4	XXXX
33.0000 -	34.0000	1	X
34.0000 -	35.0000	5	XXXXX
35.0000 -	36.0000	6	XXXXXX
36.0000 -	37.0000	8	XXXXXXXX
37.0000 -	38.0000	8	XXXXXXXX
38.0000 -	39.0000	8	XXXXXXXX
39.0000 -	40.0000	15	XXXXXXXXXXXXXXXX
40.0000 -	41.0000	19	XXXXXXXXXXXXXXXXXXXX
41.0000 -	42.0000	15	XXXXXXXXXXXXXXXX
42.0000 -	43.0000	18	XXXXXXXXXXXXXXXXXXXX
43.0000 -	44.0000	15	XXXXXXXXXXXXXXXX
44.0000 -	45.0000	13	XXXXXXXXXXXXXXXX
45.0000 -	46.0000	6	XXXXXX
46.0000 -	47.0000	8	XXXXXXXX
47.0000 -	48.0000	7	XXXXXXX
48.0000 -	49.0000	3	XXX
49.0000 -	50.0000	5	XXXXX
50.0000 -	51.0000	1	X
51.0000 -	52.0000	1	X
52.0000 -	53.0000	0	

0 VALUE(S) BELOW LOWER LIMIT
 0 VALUE(S) ABOVE UPPER LIMIT

DEFINE GRAPH INTERVAL !0

THIS PROGRAM BEST QUALITY PROGRAM
 FROM OXY APPARATUS TO DOG

172 ITEMS

MEAN = 40.09960
ST. DEVL = 6.41533

DATA AND HISTOGRAM OF THE TEMPERATURE
COEFFICIENT OF THE PERIOD BETWEEN
25 C to -50 C ppm/ C

COEFFICIENT OF SKEWNESS = -1.10259

XBAR + 1 SIGMA	46.5149	XBAR - 1 SIGMA	33.6842
XBAR + 2 SIGMA	52.9302	XBAR - 2 SIGMA	27.2669
XBAR + 3 SIGMA	59.3455	XBAR - 3 SIGMA	20.8506

11.66000	36.83000	39.04000	41.93000	44.46000
13.04000	36.95000	39.04000	41.95000	44.73000
13.26000	36.98000	39.36000	42.10000	44.85000
23.39000	37.07000	39.51000	42.11000	45.20000
25.08000	37.08000	39.66000	42.19000	45.20000
27.81000	37.14000	39.66000	42.20000	45.25000
28.20000	37.20000	39.71000	42.24000	45.25000
29.05000	37.21000	39.80000	42.28000	45.40000
30.26000	37.37000	39.93000	42.37000	45.58000
31.61000	37.39000	39.93000	42.53000	45.61000
31.69000	37.43000	40.34000	42.66000	45.75000
32.41000	37.50000	40.40000	42.80000	45.87000
32.87000	37.66000	40.51000	42.88000	45.96000
33.02000	37.88000	40.52000	42.94000	46.03000
33.36000	37.93000	40.58000	42.99000	46.79000
33.60000	37.94000	40.58000	43.11000	47.36000
33.82000	38.00000	40.61000	43.27000	47.55000
33.88000	38.07000	40.64000	43.27000	47.68000
34.10000	38.08000	40.74000	43.28000	47.69000
34.29000	38.13000	40.77000	43.30000	47.80000
34.37000	38.22000	40.83000	43.46000	47.89000
34.38000	38.27000	40.87000	43.58000	48.01000
34.72000	38.41000	41.01000	43.68000	48.02000
35.23000	38.47000	41.09000	43.73000	48.06000
35.31000	38.49000	41.40000	44.00000	48.25000
35.32000	38.56000	41.47000	44.06000	48.27000
35.62000	38.69000	41.51000	44.07000	48.30000
35.93000	38.69000	41.62000	44.08000	49.12000
36.22000	38.72000	41.78000	44.08000	50.71000
36.26000	38.76000	41.80000	44.16000	51.48000
36.32000	38.81000	41.82000	44.19000	55.14000
36.35000	38.91000	41.85000	44.28000	65.22000
36.40000	38.98000	41.88000	44.28000	
36.48000	39.00000	41.91000	44.30000	
36.70000	39.00000	41.91000	44.35000	

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DEFINE GRAPH INTERVAL 11.0
 DEFINE LOWER GRAPH LIMIT 11.0
 DEFINE UPPER GRAPH LIMIT 66.0

DATA AND HISTORICAL
 25 C to -50 C ppm/ C
 (continued)

11.0000 -	12.0000	1	X
12.0000 -	13.0000	0	
13.0000 -	14.0000	2	XX
14.0000 -	15.0000	0	
15.0000 -	16.0000	0	
16.0000 -	17.0000	0	
17.0000 -	18.0000	0	
18.0000 -	19.0000	0	
19.0000 -	20.0000	0	
20.0000 -	21.0000	0	
21.0000 -	22.0000	0	
22.0000 -	23.0000	0	
23.0000 -	24.0000	1	X
24.0000 -	25.0000	0	
25.0000 -	26.0000	1	X
26.0000 -	27.0000	0	
27.0000 -	28.0000	1	X
28.0000 -	29.0000	1	X
29.0000 -	30.0000	1	X
30.0000 -	31.0000	1	X
31.0000 -	32.0000	2	XX
32.0000 -	33.0000	2	XX
33.0000 -	34.0000	5	XXXXXX
34.0000 -	35.0000	5	XXXXXX
35.0000 -	36.0000	5	XXXXXX
36.0000 -	37.0000	10	XXXXXXXXXX
37.0000 -	38.0000	13	XXXXXXXXXXXXXX
38.0000 -	39.0000	17	XXXXXXXXXXXXXXXXXX
39.0000 -	40.0000	12	XXXXXXXXXXXXXX
40.0000 -	41.0000	12	XXXXXXXXXXXXXX
41.0000 -	42.0000	15	XXXXXXXXXXXXXX
42.0000 -	43.0000	13	XXXXXXXXXXXXXX
43.0000 -	44.0000	9	XXXXXXXXXX
44.0000 -	45.0000	14	XXXXXXXXXXXXXX
45.0000 -	46.0000	10	XXXXXXXXXX
46.0000 -	47.0000	2	XX
47.0000 -	48.0000	6	XXXXXX
48.0000 -	49.0000	6	XXXXXX
49.0000 -	50.0000	1	X
50.0000 -	51.0000	1	X
51.0000 -	52.0000	1	X
52.0000 -	53.0000	0	
53.0000 -	54.0000	0	
54.0000 -	55.0000	0	
55.0000 -	56.0000	1	X
56.0000 -	57.0000	0	
57.0000 -	58.0000	0	
58.0000 -	59.0000	0	
59.0000 -	60.0000	0	
60.0000 -	61.0000	0	
61.0000 -	62.0000	0	
62.0000 -	63.0000	0	
63.0000 -	64.0000	0	
64.0000 -	65.0000	0	
65.0000 -	66.0000	1	X
66.0000 -	67.0000	0	

0 VALUE(S) BELOW LOWER LIMIT
 0 VALUE(S) ABOVE UPPER LIMIT

DEFINE GRAPH INTERVAL 10

APPENDIX F. HISTOGRAMS OF VOLTAGE SENSITIVITY TEST

175 ITEMS

MEAN = -.00574
ST. DEV. = .00344

HISTOGRAM VOLTA~~GE~~ SENSITIVITY
(-23.5 Vdc to -30 Vdc)
(period change in 10⁻⁹ seconds)

COEFFICIENT OF SKEWNESS = .22760

XBAR + 1 SIGMA	-.0023	XBAR - 1 SIGMA	-.0092
XBAR + 2 SIGMA	.0011	XBAR - 2 SIGMA	-.0126
XBAR + 3 SIGMA	.0046	XBAR - 3 SIGMA	-.0161

-.01300	-.00900	-.00650	-.00470	-.00300
-.01260	-.00900	-.00650	-.00460	-.00280
-.01240	-.00880	-.00630	-.00430	-.00280
-.01220	-.00870	-.00620	-.00420	-.00270
-.01220	-.00870	-.00620	-.00420	-.00260
-.01210	-.00850	-.00610	-.00420	-.00250
-.01160	-.00840	-.00600	-.00420	-.00250
-.01160	-.00840	-.00600	-.00420	-.00240
-.01150	-.00830	-.00600	-.00410	-.00240
-.01140	-.00820	-.00590	-.00410	-.00240
-.01130	-.00810	-.00580	-.00410	-.00240
-.01110	-.00790	-.00580	-.00410	-.00240
-.01100	-.00790	-.00580	-.00410	-.00240
-.01080	-.00780	-.00580	-.00390	-.00230
-.01070	-.00780	-.00570	-.00390	-.00220
-.01060	-.00770	-.00570	-.00380	-.00220
-.01060	-.00770	-.00560	-.00380	-.00190
-.01040	-.00750	-.00560	-.00380	-.00190
-.01020	-.00750	-.00550	-.00370	-.00190
-.01010	-.00750	-.00550	-.00370	-.00150
-.01010	-.00740	-.00550	-.00370	-.00130
-.01000	-.00730	-.00550	-.00360	-.00120
-.01000	-.00720	-.00550	-.00360	-.00120
-.00980	-.00710	-.00540	-.00360	-.00110
-.00980	-.00710	-.00520	-.00360	-.00090
-.00980	-.00690	-.00520	-.00350	-.00080
-.00970	-.00680	-.00510	-.00350	.00010
-.00960	-.00680	-.00500	-.00350	.00020
-.00950	-.00680	-.00500	-.00350	.00030
-.00940	-.00670	-.00490	-.00340	.00030
-.00930	-.00670	-.00490	-.00340	.00110
-.00920	-.00670	-.00490	-.00330	.00140
-.00920	-.00650	-.00480	-.00330	.00160
-.00920	-.00650	-.00480	-.00320	.00260
-.00910	-.00650	-.00480	-.00320	.00770

DEFINE GRAPH INTERVAL !.002
DEFINE LOWER GRAPH LIMIT !-.0132
DEFINE UPPER GRAPH LIMIT !.008

-.0132 -	-.0112	11	XXXXXXXXXXXX
-.0112 -	-.0092	20	XXXXXXXXXXXXXXXXXXXX
-.0092 -	-.0072	27	XXXXXXXXXXXXXXXXXXXXXXXXXXXX
-.0072 -	-.0052	38	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
-.0052 -	-.0032	44	XX
-.0032 -	-.0012	23	XXXXXXXXXXXXXXXXXXXXXXXXXXXX
-.0012 -	.0008	7	XXXXXXX
.0008 -	.0028	4	XXXX
.0028 -	.0048	0	
.0048 -	.0068	0	
.0068 -	.0088	1	X

0 VALUE(S) BELOW LOWER LIMIT
0 VALUE(S) ABOVE UPPER LIMIT

DEFINE GRAPH INTERVAL !0

75 ITEMS

MEAN = .00944 HISTOGRAM OF VOLTAGE SENSITIVITY
 ST. DEV. = .00325 (-23.5 Vdc to -17.0 Vdc)
 (period change in 10⁻⁹ seconds)
 COEFFICIENT OF SKEWNESS = -.82801

XBAR + 1 SIGMA	.0127	XBAR - 1 SIGMA	.0062
XBAR + 2 SIGMA	.0159	XBAR - 2 SIGMA	.0029
XBAR + 3 SIGMA	.0192	XBAR - 3 SIGMA	-.0003

-.00470	.00680	.00870	.01060	.01250
.00040	.00680	.00880	.01070	.01250
.00070	.00700	.00890	.01070	.01250
.00110	.00700	.00890	.01070	.01260
.00230	.00710	.00910	.01080	.01260
.00280	.00710	.00920	.01080	.01260
.00350	.00720	.00920	.01080	.01270
.00350	.00720	.00920	.01080	.01270
.00360	.00730	.00930	.01080	.01270
.00370	.00740	.00940	.01090	.01280
.00410	.00750	.00940	.01090	.01280
.00460	.00750	.00950	.01100	.01290
.00490	.00760	.00950	.01100	.01290
.00520	.00770	.00960	.01100	.01300
.00530	.00780	.00990	.01100	.01300
.00540	.00780	.00990	.01120	.01310
.00560	.00790	.00990	.01120	.01320
.00570	.00790	.01000	.01120	.01320
.00570	.00800	.01000	.01130	.01340
.00580	.00810	.01010	.01130	.01350
.00590	.00820	.01020	.01150	.01350
.00590	.00840	.01020	.01160	.01360
.00590	.00840	.01020	.01160	.01370
.00600	.00840	.01030	.01170	.01380
.00610	.00840	.01030	.01170	.01380
.00610	.00840	.01030	.01180	.01390
.00630	.00840	.01040	.01190	.01420
.00640	.00850	.01040	.01190	.01430
.00640	.00850	.01050	.01200	.01440
.00640	.00850	.01060	.01210	.01440
.00640	.00850	.01060	.01220	.01460
.00640	.00860	.01060	.01230	.01470
.00640	.00860	.01060	.01230	.01480
.00660	.00860	.01060	.01240	.01480
.00670	.00870	.01060	.01240	.01490

DEFINE GRAPH INTERVAL !.002
 DEFINE LOWER GRAPH LIMIT !-.005
 DEFINE UPPER GRAPH LIMIT !.015

-.0050 -	-.0030	1	X
-.0030 -	-.0010	0	
-.0010 -	.0010	2	XX
.0010 -	.0030	3	XXX
.0030 -	.0050	7	XXXXXXX
.0050 -	.0070	24	XXXXXXXXXXXXXXXXXXXXXXXXXXXX
.0070 -	.0090	37	XXXXXXXXXXXXXXXXXXXXXXXXXXXX
.0090 -	.0110	42	XXXXXXXXXXXXXXXXXXXXXXXXXXXX
.0110 -	.0130	37	XXXXXXXXXXXXXXXXXXXXXXXXXXXX
.0130 -	.0150	22	XXXXXXXXXXXXXXXXXXXX
.0150 -	.0170	0	

0 VALUE(S) BELOW LOWER LIMIT
 0 VALUE(S) ABOVE UPPER LIMIT

DEFINE GRAPH INTERVAL 10

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**APPENDIX G. FAILURE ANALYSIS REPORT ON TEMPERATURE
CYCLE AND HIGH TEMPERATURE STORAGE FAILURES**

Honeywell

DEFENSE SYSTEMS DIVISION

FAILURE ANALYSIS LAB FAILURE ANALYSIS REPORT



DATE 5/16/78	PROJECT XM587	MALFUNCTION/F&A REPORT NUMBER	REPORT NUMBER 69296
PART NAME 10KHZ TAB Hybrid Microcircuit Oscillator	DRAWING/PART NUMBER 11726813	GENERIC PART/NUMBER	
SERIAL NUMBER	MANUFACTURER Honeywell DSD	DATE CODE	

1. BACKGROUND

2. ANALYSIS PROCEDURE

3. CONCLUSIONS

4. RECOMMENDATIONS
(OPTIONAL)

5. EQUIPMENT USED
(OPTIONAL)

BACKGROUND

Four Tape Automatic Bonded (TAB) hybrid microcircuit oscillators were submitted for failure analysis. Three of the TAB hybrid microcircuit oscillators exhibited excessive period (T) drift during temperature cycles testing (-55°C to $+125^{\circ}\text{C}$), and one TAB hybrid microcircuit oscillator exhibited excessive period drift during high temperature storage testing ($+125^{\circ}\text{C}$ for 500 hours). The TAB hybrid microcircuit oscillators were inadvertently placed in the temperature cycle test where the extreme temperatures were $+125^{\circ}\text{C}$ and -55°C . Specification requirements, HDL Dwg 11726813, are $+71^{\circ}\text{C}$ to -55°C . Subsequent temperature cycle testing of an additional 25 TAB hybrid microcircuit oscillators with $+71^{\circ}\text{C}$ and -55°C as the extreme temperature limits did not reveal any failures. The 22 TAB hybrid microcircuit oscillators which passed the $+125^{\circ}\text{C}$ to -55°C temperature cycle test were exposed to an additional 8 temperature cycles and no other failures were noted.

ANALYSIS

The TAB hybrid microcircuit oscillator period drifts are shown in Table I.

TABLE I
PERIOD DRIFTS DURING ENVIRONMENTAL TESTING

SERIAL NUMBER	INITIAL T (10^{-6} sec)	POST ENVIRONMENT T (10^{-6} sec)	ΔT (10^{-6} sec)	ENVIRONMENTAL TEST
3	99.2337	99.8654	.6317	Temperature Cycle
14	97.0150	98.6575	1.6425	Temperature Cycle
29	98.5339	100.8904	2.3565	Temperature Cycle
86	98.5515	99.0540	.5025	High Temperature Storage

The allowable period drift during temperature cycle and high temperature storage tests is $\pm 250 \times 10^{-9}$ seconds. Electrical measurements revealed typical supply currents ranging from 1.78 mAdc to 1.98 mAdc.

All oscillator failures exhibited the same failure mechanism. Visual examination subsequent to decapsulation revealed lifted and fractured thick film dielectric and resistive film in R1. The cracking and flaking of the resistive film occurred at and/or near the termination (low fire silver thick film conductor) which goes to the amplifier output. The epoxy was removed mechanically. Lifting the silicone barrier layer over R1 revealed the thick film dielectric and thick film resistive element were not properly adhering to the substrate. Reference Photograph 1 and 2. A discrete resistor (33.982k Ω) was substituted for R1 to verify that all period drifts were caused by R1

increasing in value due to microfractures in the resistive film. Table II shows the initial period and the period after substituting the discrete resistor on the hybrid microcircuit oscillator substrate.

TABLE II
PERIOD MEASUREMENTS AFTER SUBSTITUTING
A DISCRETE RESISTOR FOR R1

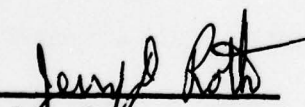
SERIAL NUMBER	INITIAL (10^{-6} sec)	POST SUBSTITUTION OF R1 (10^{-6} sec)
3	99.2337	99.2950
14	97.0150	97.1160
29	98.5339	98.6353
86	98.5515	98.7766

Electrical measurements after substitution of the discrete resistor for R1 verified all period drifts resulted from R1 increasing in value. The exact cause of the lifted and fractured thick film dielectric and resistive film is unknown. However, it was apparent that the failure mechanism was susceptible to an excessive thermal gradient.


CONCLUSION

Four TAB hybrid microcircuit oscillators failed due to excessive period drifts during temperature cycle and high temperature storage tests. The excessive period drift resulted from R1, one of the $34k\Omega$ resistors in the Twin-T network increasing in value. Visual examination revealed lifted and fractured thick film dielectric and resistive film. The cause of the failure mechanism is unknown.

Prepared by


J.D. Roth
Failure Analyst

Approved by


D.A. Tabor
Reliability Engineer

FAILURE ANALYSIS REPORT

Report Number 69296

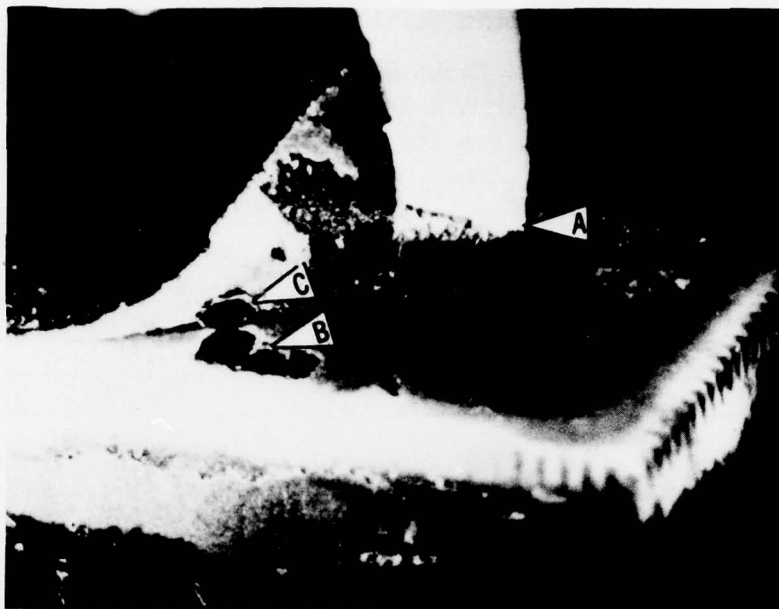


Photo #1 (Unit #86)

Magnification 18.5X

(A) shows silicone barrier layer held away from substrate by (yellow) tape.

(B) shows area where resistive film was removed from R1.

(C) shows a portion of the resistive film attached to the silicone barrier layer.

FAILURE ANALYSIS REPORT

Report Number 69296

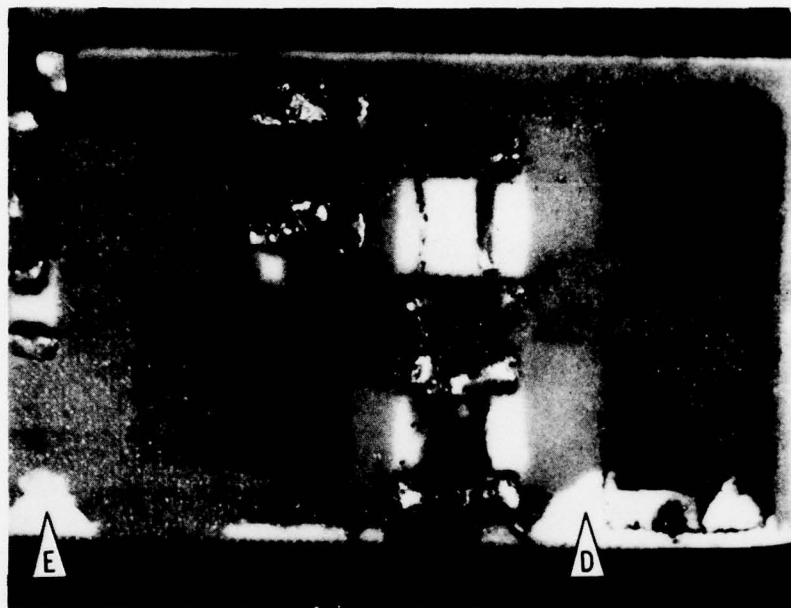


Photo #2 (Unit #14)

Magnification 7.5X

(D) shows the resistive film and metal track missing from substrate.

(E) shows area where metal track is missing from substrate.

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